Audit of the BLM LHC system

Beam loss interface to machine protection
and energy distribution

The BLECS combiner
and survey card

Functional test bench
for the BLECF and BLECS

Jonathan Emery
10 June 2008

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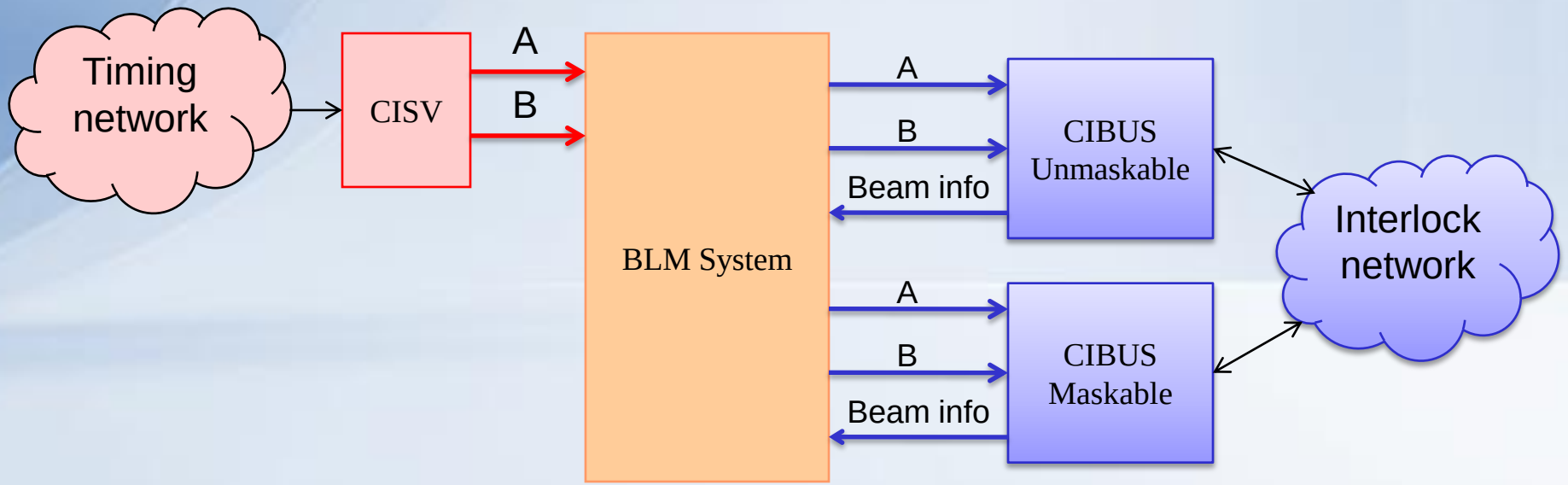
Outline

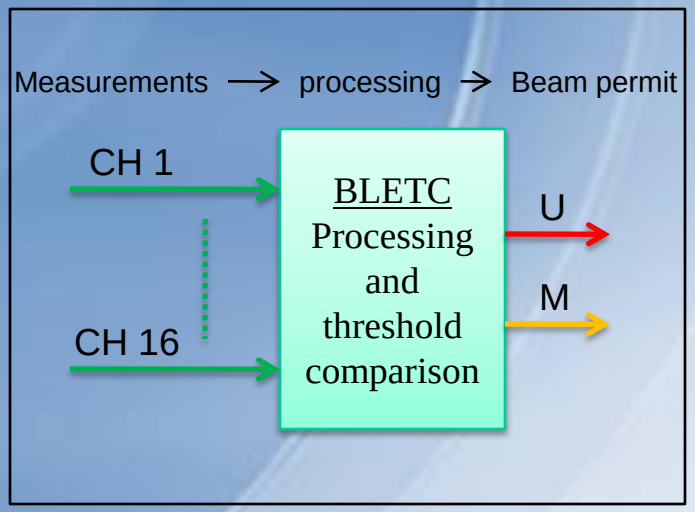
- **Overview**
- **Beam permit hardware**
- **Beam permit check**
- **Beam energy**

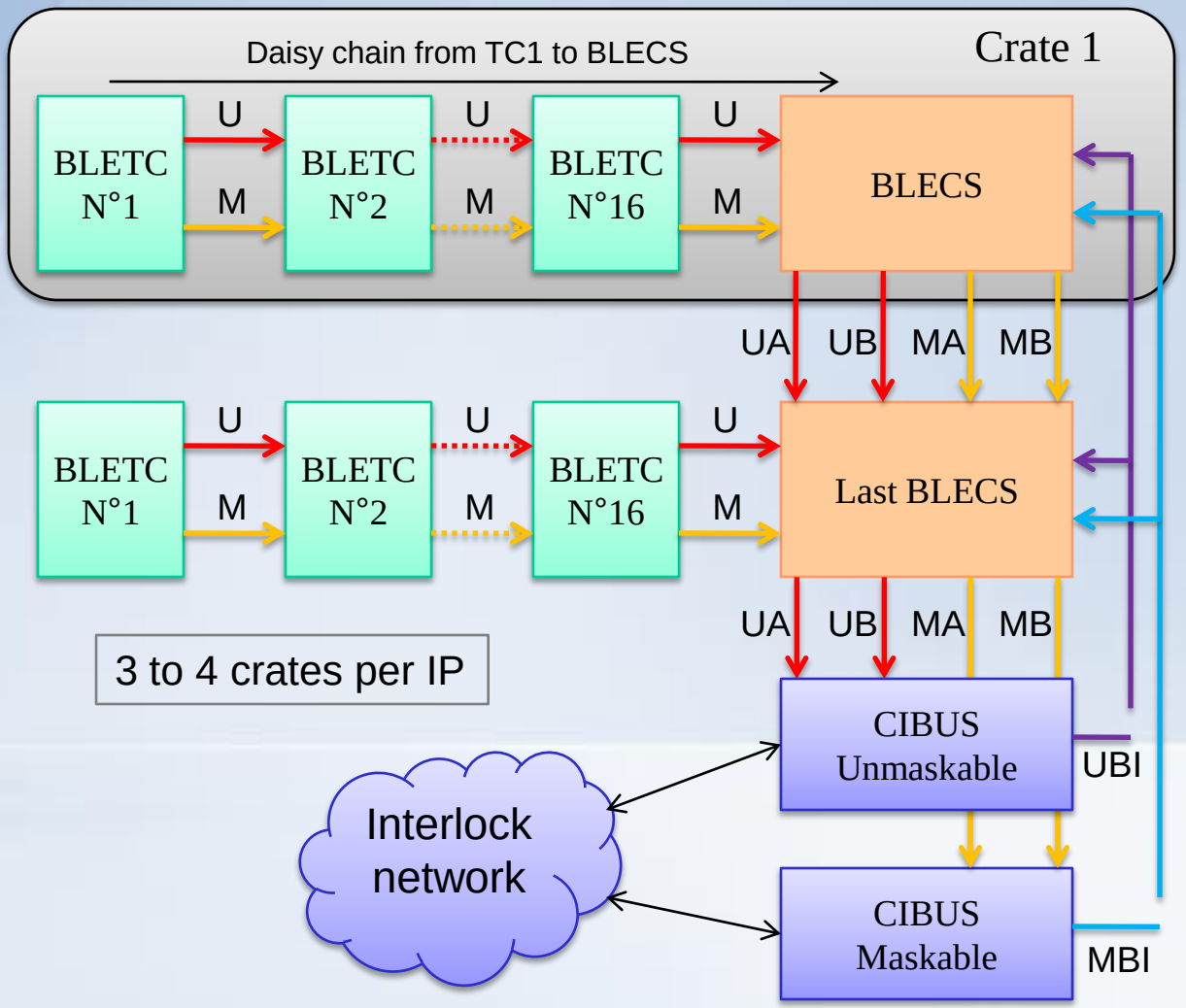
Overview for one IP

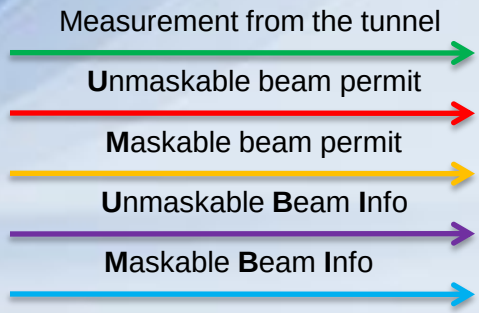
- The BLM receive the energy through a redundant link from the CISV
- The beam permit signals, maskable and unmaskable, are send to the CIBUS with 2 redundant lines (A and B)



Beam permit signal path

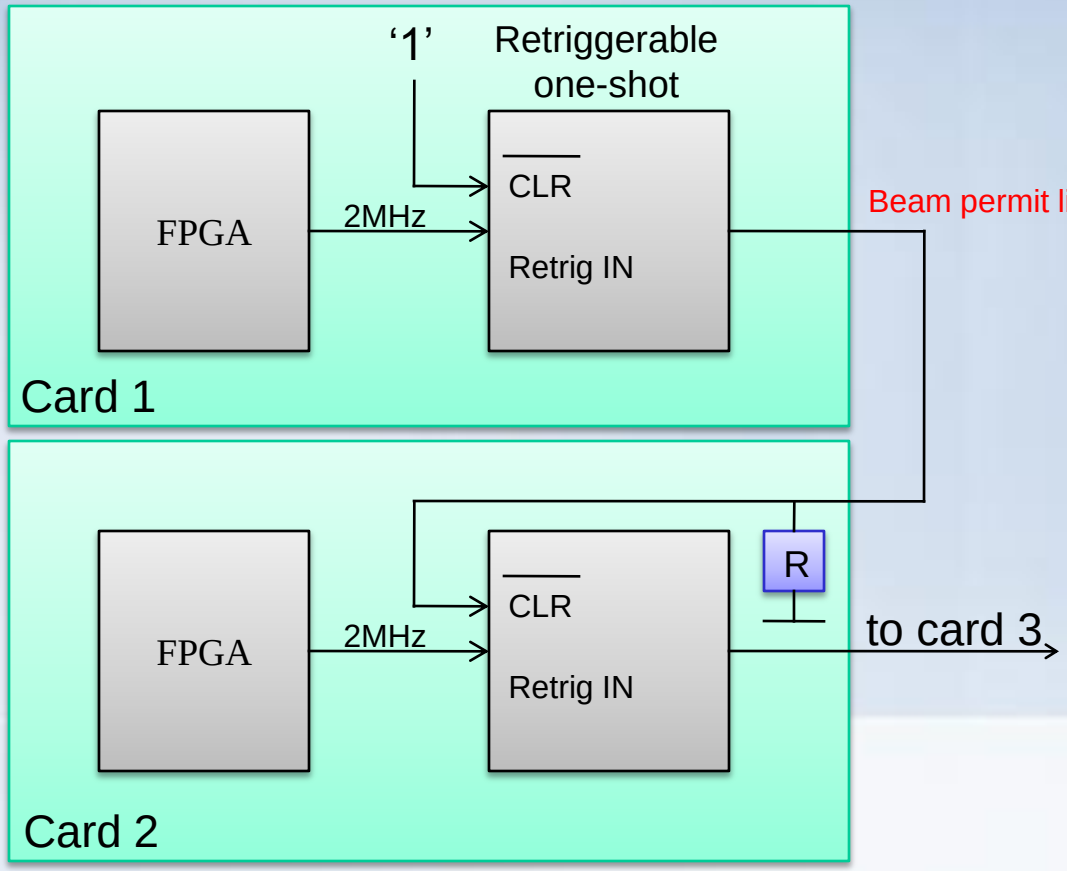






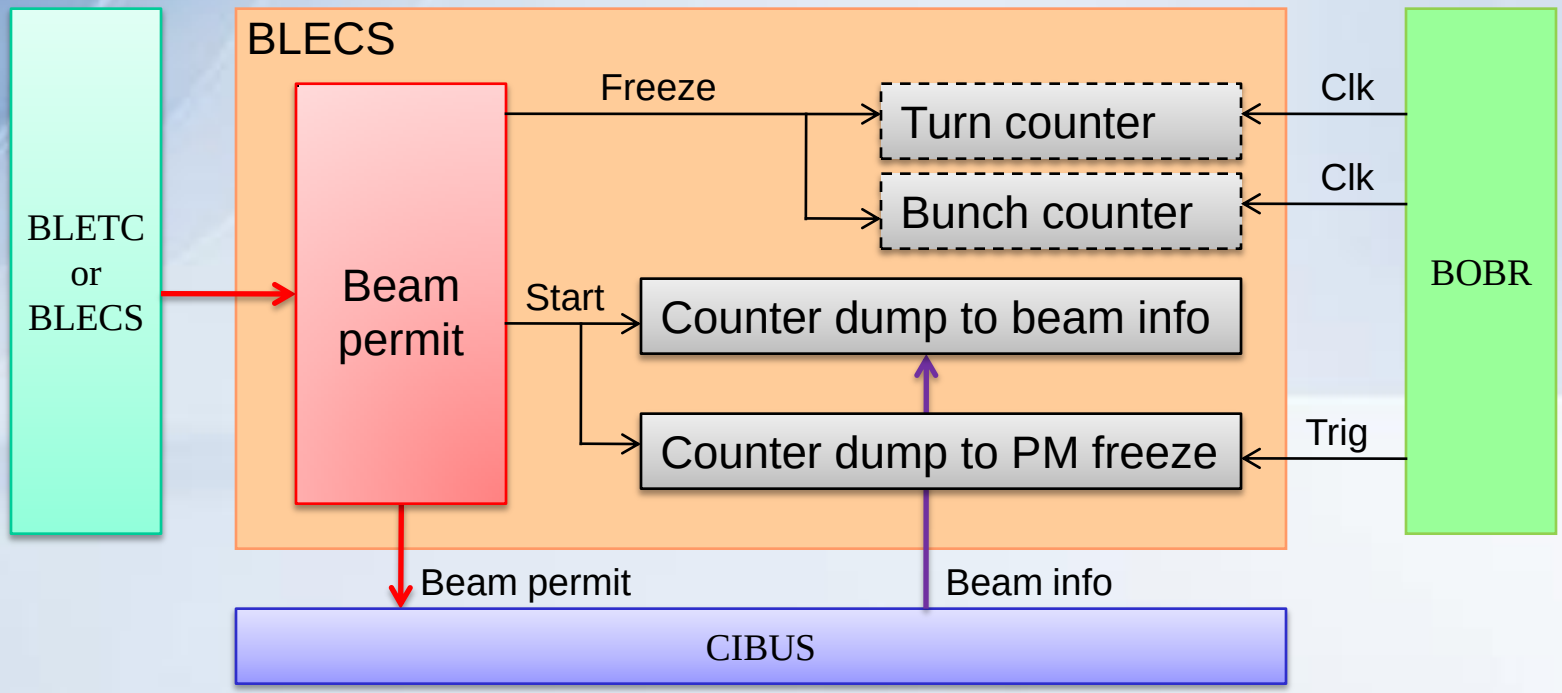
Beam permit daisy chain principle

- The FPGA provide a clock line to the one-shot chip
- The CLR input is used to combine the signal from the previous card
- A pull-down resistor is used in case of a broken wire or a unwanted board removal
- Same principle for the 2 links
  Inside the crate (BLETC to BLETC)
  Between the crates (BLECS to BLECS)



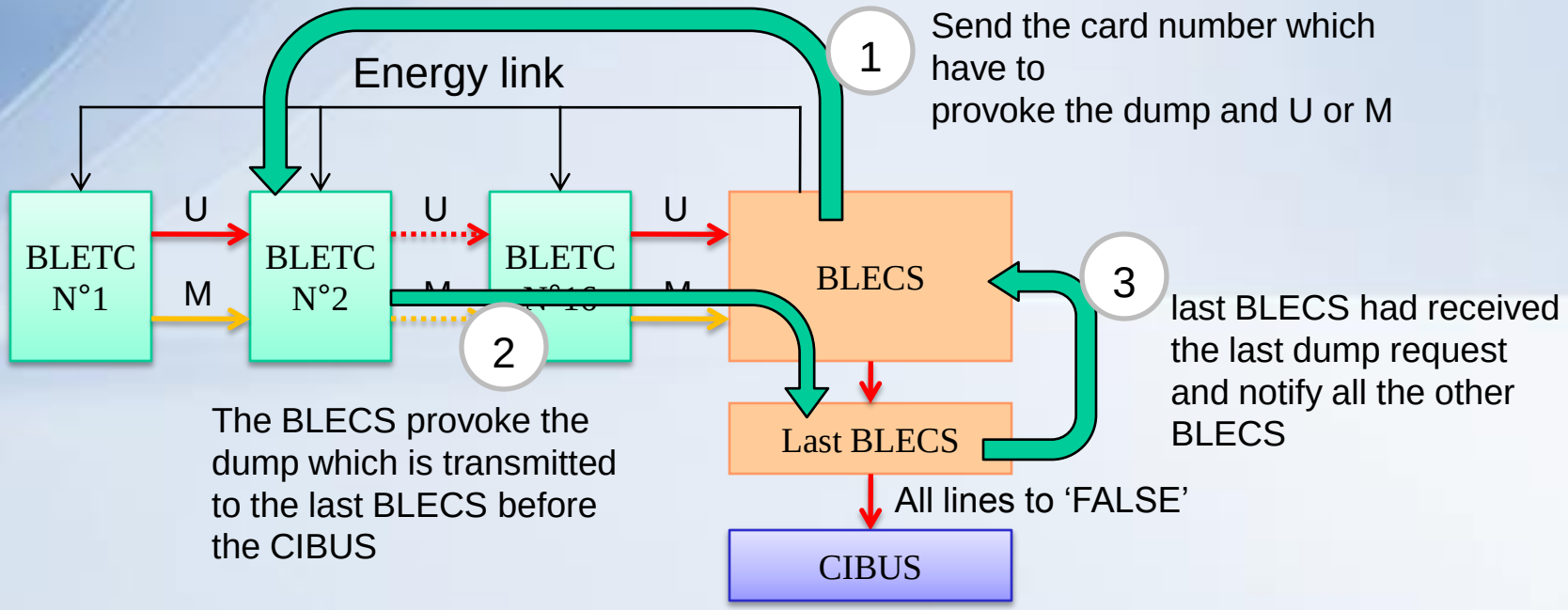
Beam dump request time stamping

- A counter starts when the beam permit goes down, stops when the PM freeze trigger arrives. The CPU calculate the time stamp with the PM freeze arrival time and this counter (1µs accuracy).
- A status tells is the beam info had arrived after a dump request and gives the delay between this 2 events.



Beam permit test procedure1

- Tests the beam permit lines (BPL) inside the crate
- Tests the BPL between the crates (on the same IP)
- Test results are saved in the database



Beam permit test procedure 2 (proposal)

Tests the BPL from the last crate to the CIBUS

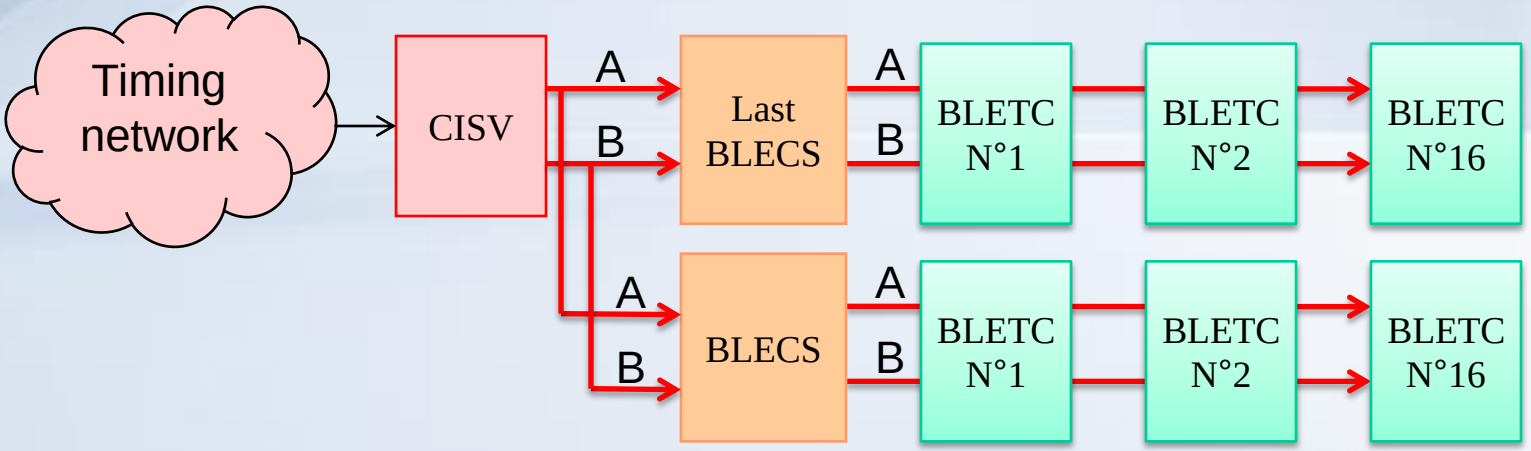
1. Request from outside system (interlock system) to enter in test
2. BLM system waits for the beam info to be 'False' (U & M)
   Enter in the test mode after a predefined time
3. Then it is possible to force only one BPL (A or B) to 'true'
4. The BLM system return to normal state when the result is given to the BLECS

The beam permits goes to normal operation state only if the test is successful

- Control of the BPL by an outside system only if the BLM system is in "test mode"
- The BLM system can only go to "test mode" if the beam info is "False"
- Only one line (A or B) can be "True". The other one stay "False"

Beam energy

- The beam energy arrives from the timing system to the CISV located on the one crate of each IP (blmr)
- The CISV distribute the energy to all BLECS of the point (3 to 4 crates) in parallel through the cables between the crates.
- The integrity of the link is continuously checked and errors are counted and saved in the logging database.
- Conversion is done from 16bits to 5bits levels (32 levels of the BLM system). This conversion (linear) is hardcoded inside the FPGA of the BLECS

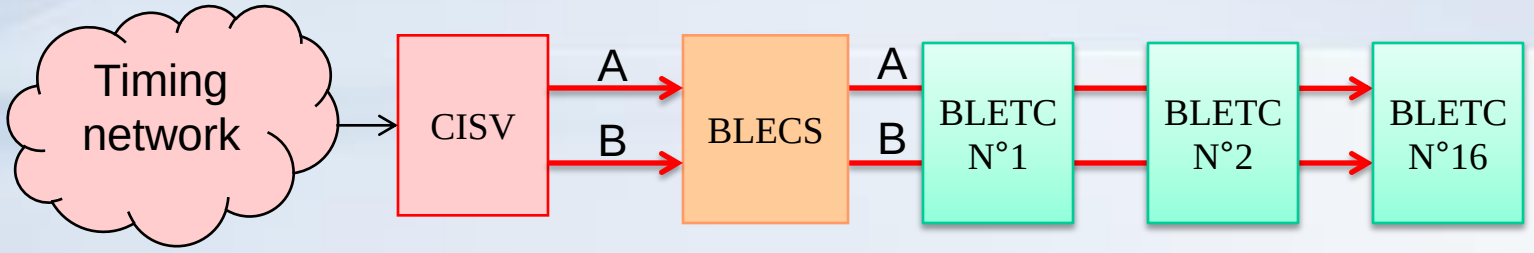


Beam energy link

- New energy value every 100ms
- The energy frames are transmitted every ms
  (the energy value is repeated between new values)
- Uses a serial link, 1MHz bit rate, Manchester encoding
- The frame is 32 bits long and content:
  LHC energy header (“1001“)
  Spare bits (”000”)
  Toggle bit expected to have a transition every 100ms
  Energy value (16 bits)
  CRC (8 bits)

Toggle bit expected to have a transition every 100ms → Error counters to the DB

CRC (8 bits) → Error counters to the DB



Audit of the BLM LHC system

The BLECS combiner and survey card

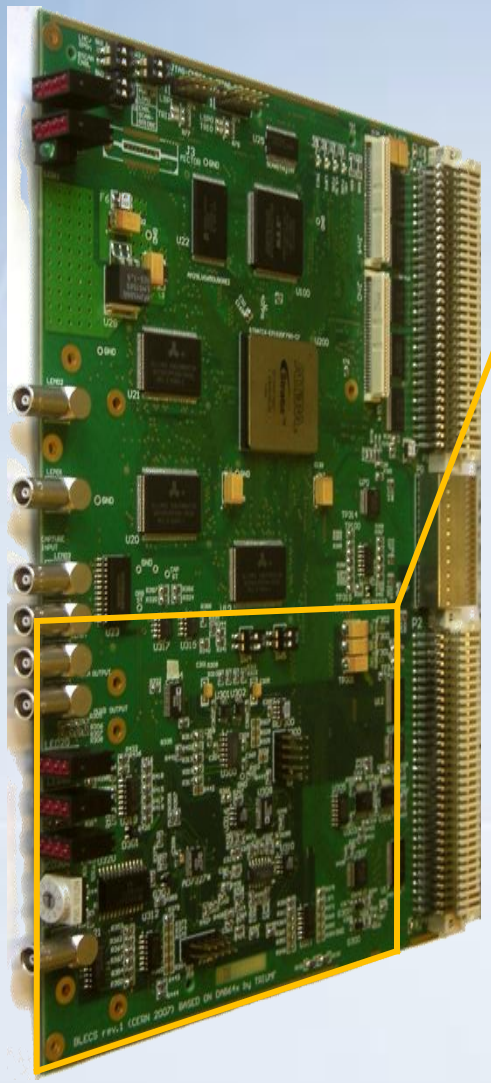
Jonathan Emery
10 June 2008

Outline

- **Hardware**
- **Crate overview**
- **Beam energy**
- **Beam permit**
- **High voltage control**
- **Voltages survey**
- **Tests**

Hardware

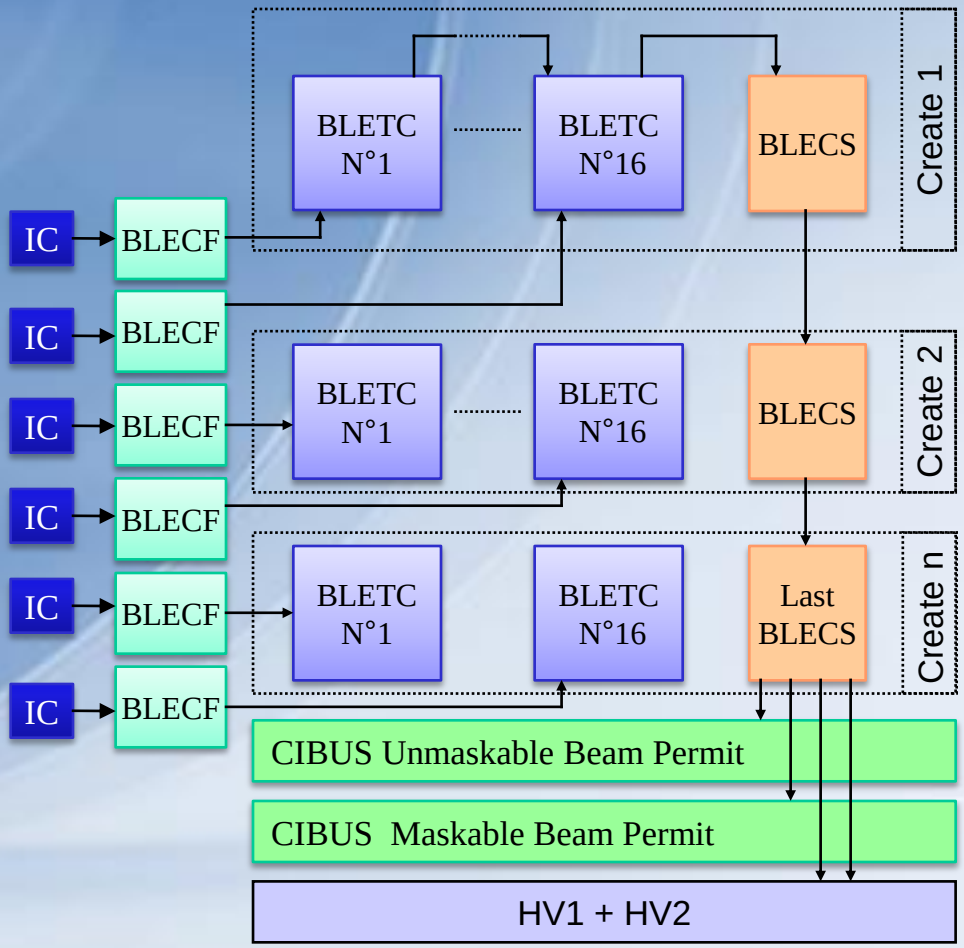
- Based on DAB card
  => VME 64x
  => Stratix 40k
  => SRAM memory
  => One site code update
  => Specific BI signals on P0
- Reuse of existing material
  => FPGA code for
  VME
  Serial number chip
  Flash memory
  => Flash programming



Combiner features added

- Beam permit
  => Daisy chain between crates
  => Beam Interlock
  CIBUS interface
- Interface to high voltage PS
  DAC for control
  ADC for monitoring
- Monitoring VME PS
  for specific behavior (ripples)
- Crate interconnections for
  test of the BLM system

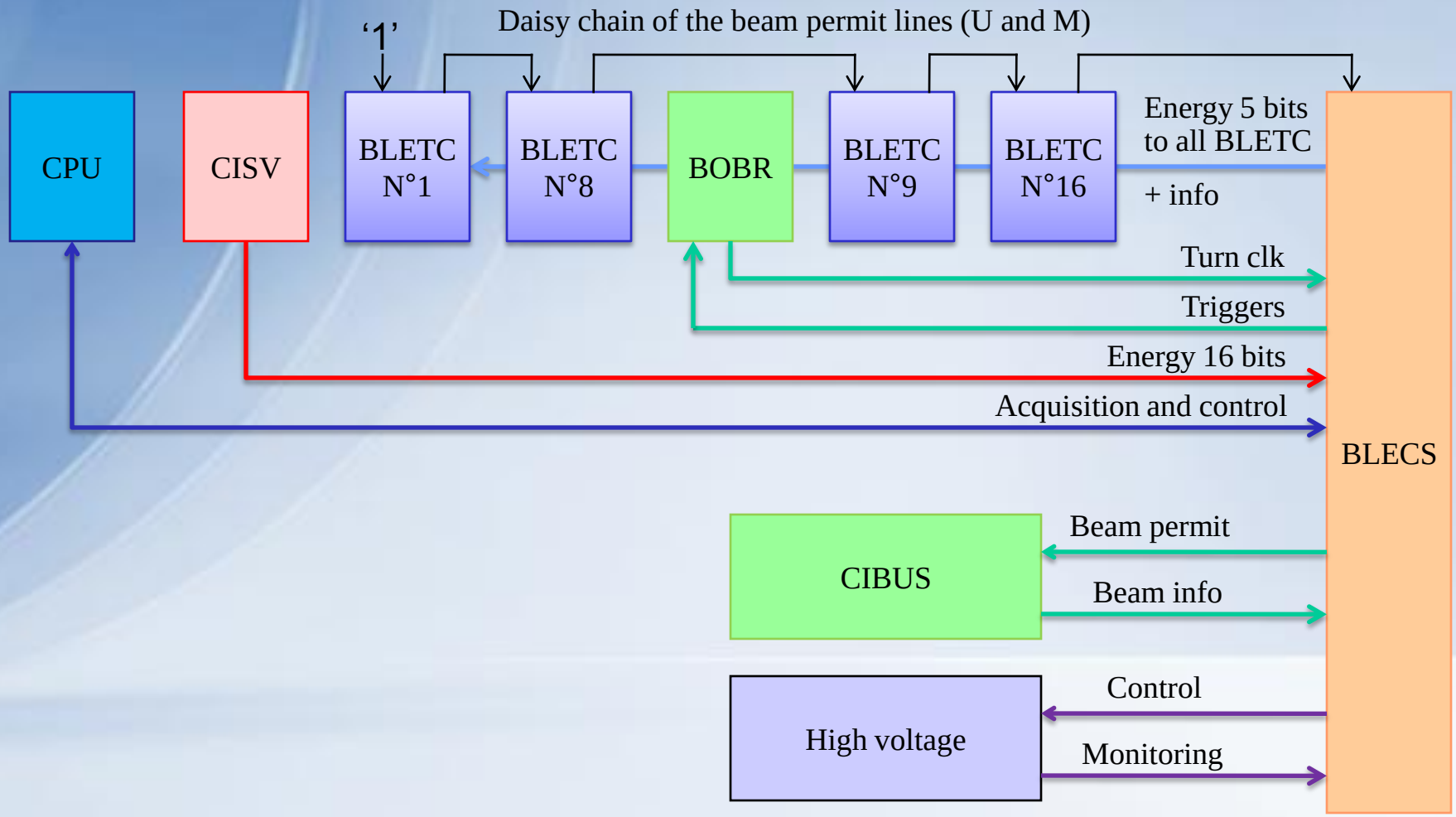
Hardware



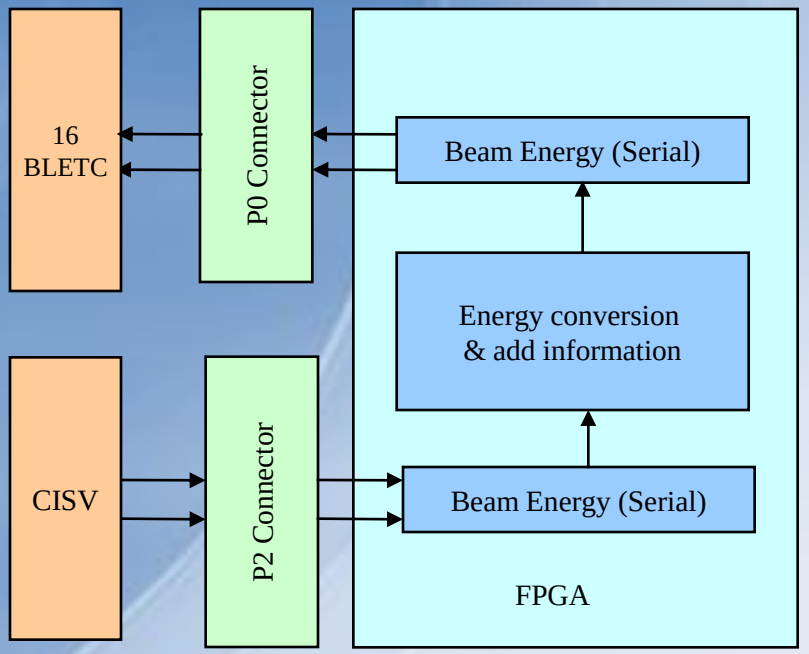
- Interconnection between crates (1 to 4)
- Beam permit: same connection between BLECS than between BLECS and CIBUS
- Last BLECS (before the CIBUS) control the HV but all can read the monitoring of this voltage.
- Beam energy distribution from last crate to all the others

IC Ionization chamber
BLECF Tunnel card for acquisition
BLETC Processing card
BLECS Combiner card
CIBUS Interlock interface
HV High Voltage power supply

Crate overview



Beam energy



- Serial reception with redundant channels (A and B)
- Continuous check for:
  Frame reception, CRC error, timeout frame, time out toggle bit
- Translation 16 bits to 5bits+1bit(error signal). Hardcoded conversion table
- Substitution of the original value by any value (in test mode only)
- Additional information on the reminded free bits
- Serial transmission to the 16 TC receivers in parallel

CRC error or timeout A	CRC error or timeout B	Toggle bit timeout	source used for the energy	Action	Comment
0	0	0	A	-	Normal operation
1	0	0	B	Increase counter CRC error A	
0	1	0	A	Increase counter CRC error B	
1	1	0	-	Previous beam energy value used	
x	x	1	Highest Energy "FFFF" & error bit '1'	Increase counter Toggle bit timeout	The timeout is 110% of the normal time between the energy values

Beam energy

CISV transmission specification
1. LHC energy header => "1001“
2. ”000”
3. Toggle bit → Toggle bit time out check (errors counter)
4. Energy value (16 bits) → Energy value (16 bits)
5. CRC (8 bits) → CRC check (errors counter)

Conversion + additional information & control

	Beam Energy (0 to 31) [5 bits]	Error bit [1 bit]	SofResetTC [1bit]	System under Test	Unmaskable Beam Info [1 bits]	Maskable Beam Info [1 bits]	BPL Unmaskable test activation [1 bit]	BPL Maskable test activation [1 bit]	Beam Permit Line test TC Card Number [4 bits]
Bit position	[15..11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3..0]
Broken link state*	31 (highest)	1	0	0	1	1	0	0	0

* Applied when both transmission are broken.

Information from the CIBUS

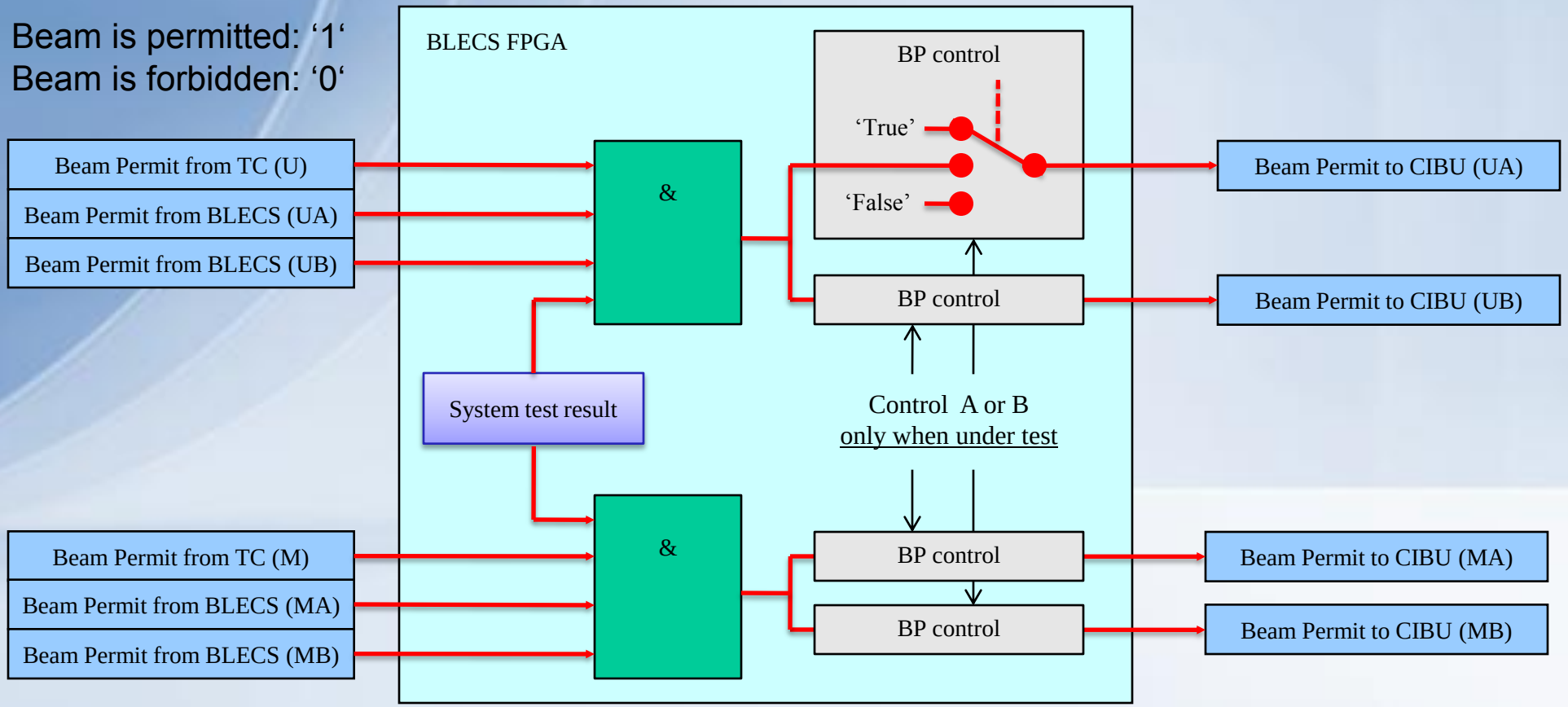
Used to provoke beam dump to TC individually (during test)

To 16 BLETC in parallel

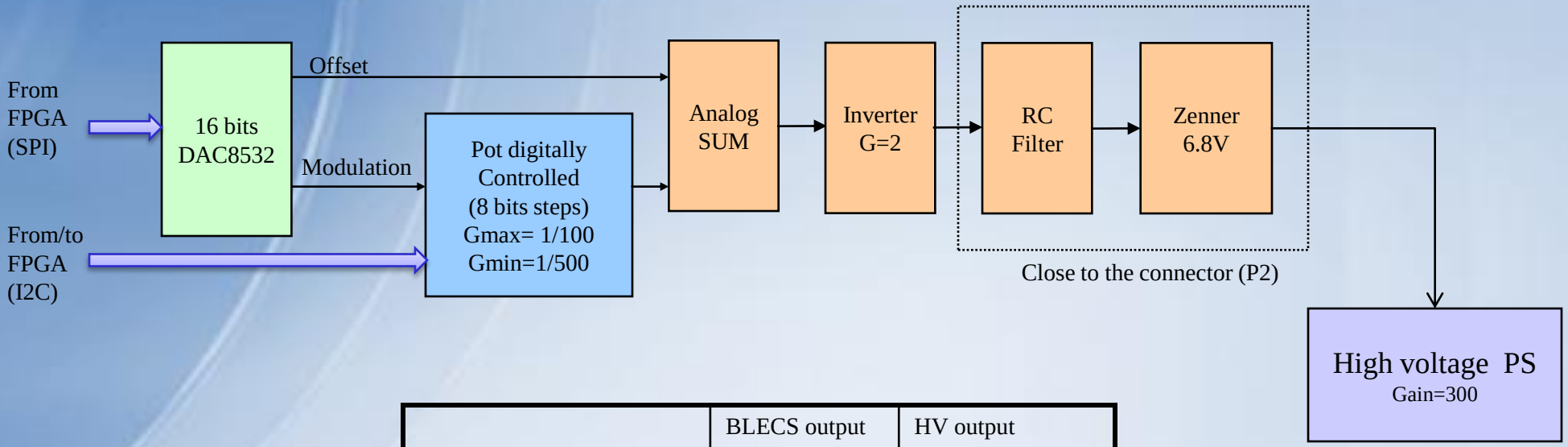
BLECS transmission specification
1. ”10010000” header (8 bits)
2. Composite data (16 bits)
3. Toggle bit + ”000” (4 bits)
4. CRC (4 bits)

Beam permit

The beam permit signal is travelling on the VME P0 connector from the first BLETC (1) to the last BLETC (16) and then to the BLECS with a daisy chain link.
One for the unmaskable and one for the maskable



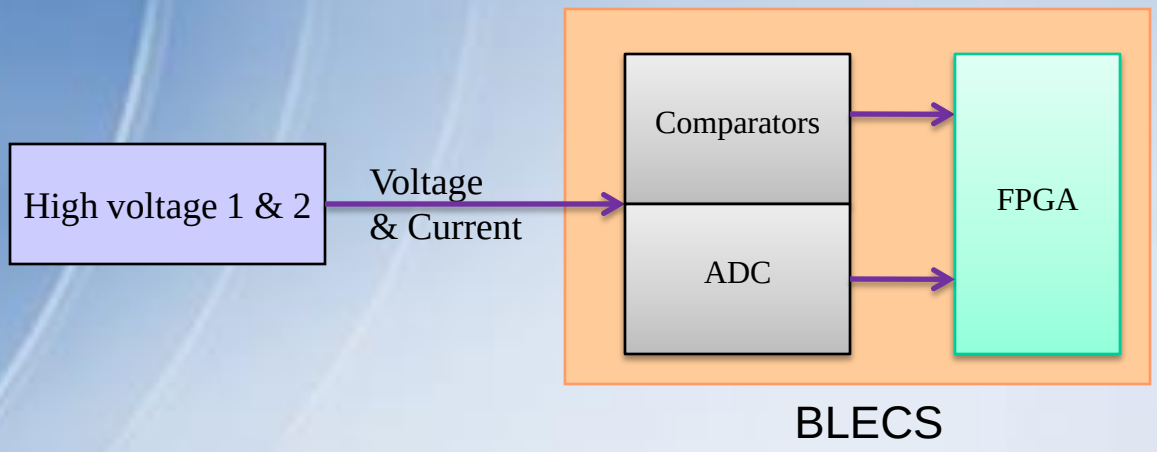
High voltage control



	BLECS output	HV output
Voltage step	0.153 mV	45.8 mV
Voltage range	6.8 V	2040 V
Modulation range peak-peak (theoretical values)	78nV to 200mV	23µV to 60V

Ionization chambers high voltage controlled by 0-10V signal
Analog sum between the working voltage 5V-6.8V and a small modulation (16mV)

High voltage monitoring



Comparators	LOW	HIGH
Voltage	< 500V	> 2100V
Current	< 0.5mA	> 18mA

	BLECS input	@ the HV [V]	@ the HV [I]
ADC maximum resolution (DC) 24 bits	0.6 mV	0.18 mV	1.2 nA
Measured noise (over 10h)	1.61 mV	0.5V @ 1505V	40mA @ 1.3mA

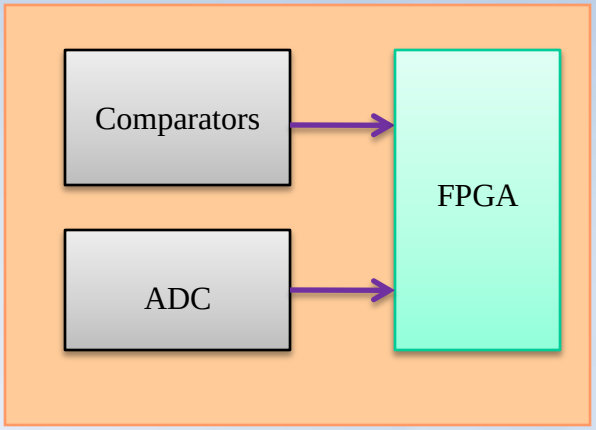
The high voltage power supplies have analog output monitors to view the voltage and current levels, these signals are digitalized with an ADC. There are also comparators checking the levels.

Low voltage monitoring

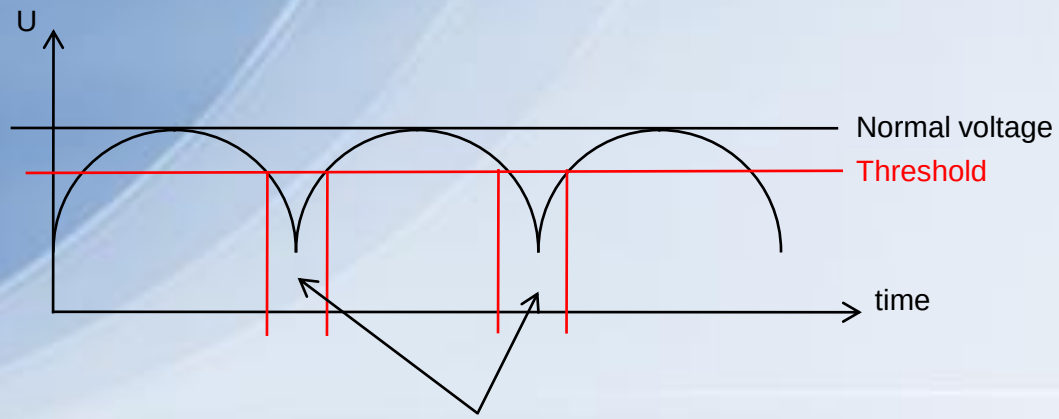
The voltages on the combiner are monitored since some ripples due to ageing were observed on previous BLM system.

<u>There are 2 ways to observe it:</u>

- With the comparators connected to counters
- With ADC values (~5kHz), the FPGA calculate the delta (max – min) when this value increase, its means there is ripples.



BLECS



Under the threshold value:
the comparator notify it, the counter is increasing by one
<u>OR t</u>he counter is measuring the time below

	Digitalization	comparator
5V (VME)		
3V3 (VME)		
±12V (VME) not used on the board		
5V (P0 Analog)		
15V (P0 Analog)		
-15V (P0 Analog)		
5V (Reference of the DAC)		
10V (HV comparator ref 2x)		

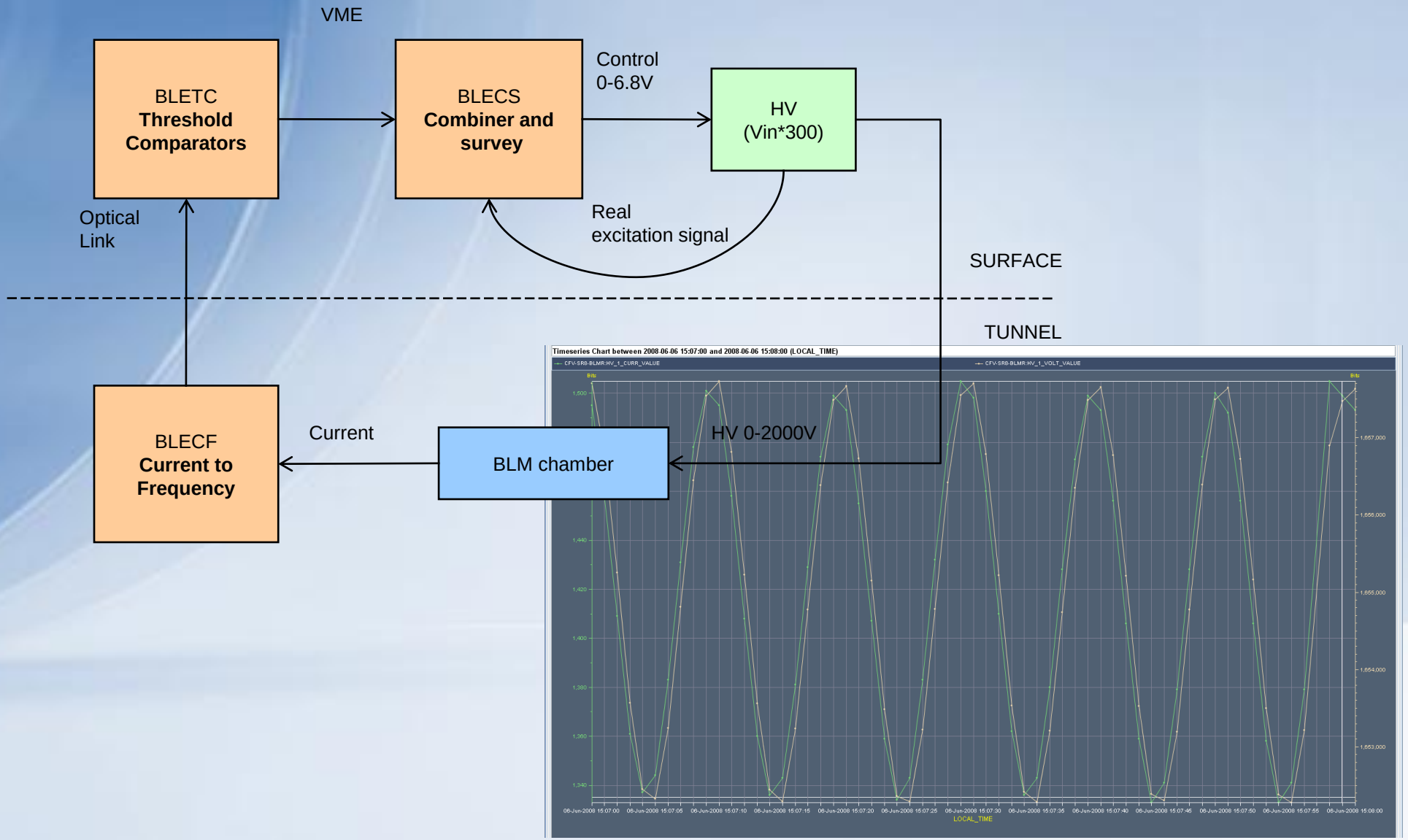
Tests

- System test includes the most important test below
  Consistency, BPTC, HVLF
- Related to the thresholds and parameters
  Consistency Check of the LSA parameters inside the electronic
- Related to the beam interlock
  BPTC Check of the beam dumping capability on each BLETC
  BPBIS Check of the beam dumping capability of the BLECS to the BIS
- Related to the high voltage
  HVLF Check of the connection from HV to IC to BLETC
  HVCFC Check of the BLECF capability to add 100pA on all channels (1650)
  HVRDAC Reset of the BLECF current compensation (related to 10pA test) (1800)
  HVRGOH Reset of the GOH on the BLECF (optical link to the surface (2000)

Test “SYSTEM TEST”

- The “SYSTEM TEST” should be done regularly
- A timer on the BLECS is requesting this test with 2 level of priority: Normal and High
- When the High priority request is raised, at the next dump, the beam permit lines are forced “False” and a system test should be started and be successful in order to go back to normal state
- The system test includes the following tests:
  Consistency
  HVLF modulation
  BPTC (beam permit lines until the last BLECS)

Tests: HVLF (HV modulation)



Tests request matrix

	Internal Timer	User	Expert
Consistency*	x	x	x
BPTC Beam Permit Lines	x	x	x
HVLF HV Modulation	x	x	x
BPBIS*		x	
HVCFC HVRDAC HVRGOH			x
Manual actions			x

All these tests are part of the SYSTEM TEST

* The result decision is done externally and is written on the combiner (Passed/Failed) in order to gives the beam permit again.

BLECS overview

- Links the BLM system to the Interlock system
- Receives and translates the energy
- Control the detectors' HV
- Request periodic test
- Test parts of the BLM system
  All BPL except the one to the CIBUS
  The connections of all the installed detectors (HVLF)
  Initiate test related to HV level
- Blocks the BPL if a test failed
  System test, Consistency, BPBIS

Audit of the BLM LHC system

Functional test bench for the BLECF tunnel card and BLECS combiner and survey card

Jonathan Emery
10 June 2008

Outline

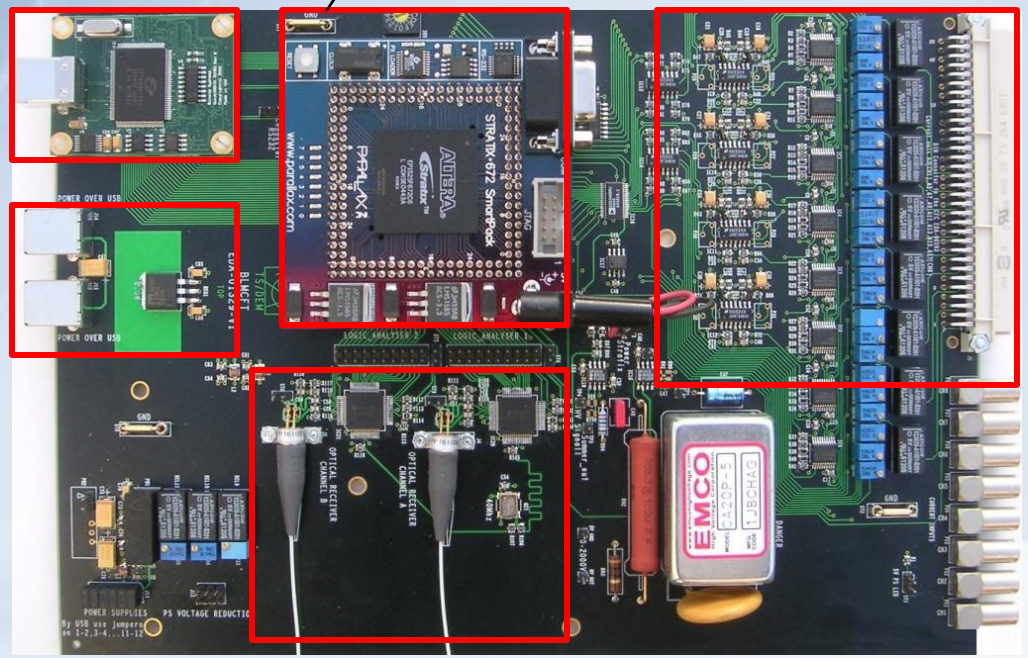
- **BLECF test bench**
  - **Hardware**
  - **Software**
  - **Functional test**
- **BLECS test bench**
  - **Software**
  - **Functional test**
- **Summary**

BLECF test bench hardware board

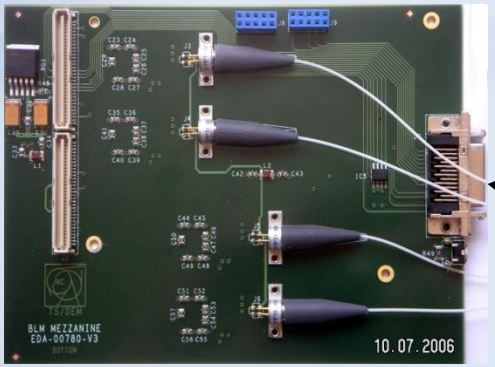
FPGA module (parallax) with custom code including the BLETC processing

USB module "Quick USB"

Power the board from the USB



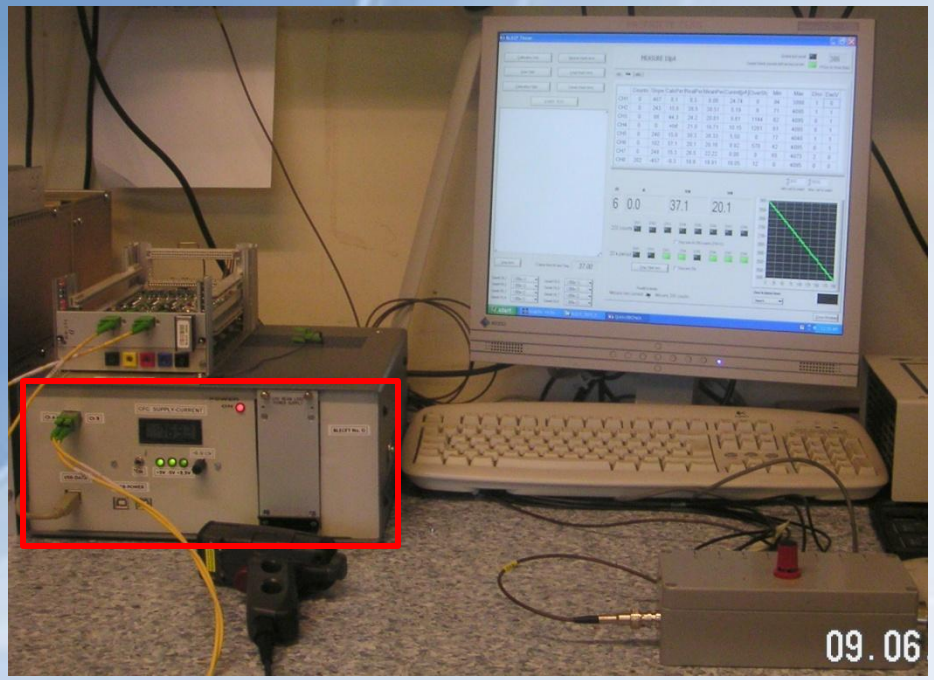
Current source circuits to feed the BLECF 10pA to 1mA on 8 channels



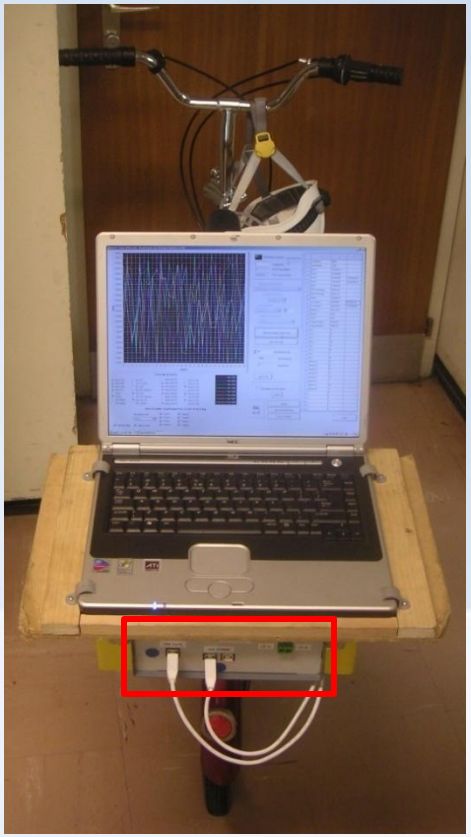
Optical receiver bloc from the BLM mezzanine

BLECF test bench

Lab version



Tunnel version



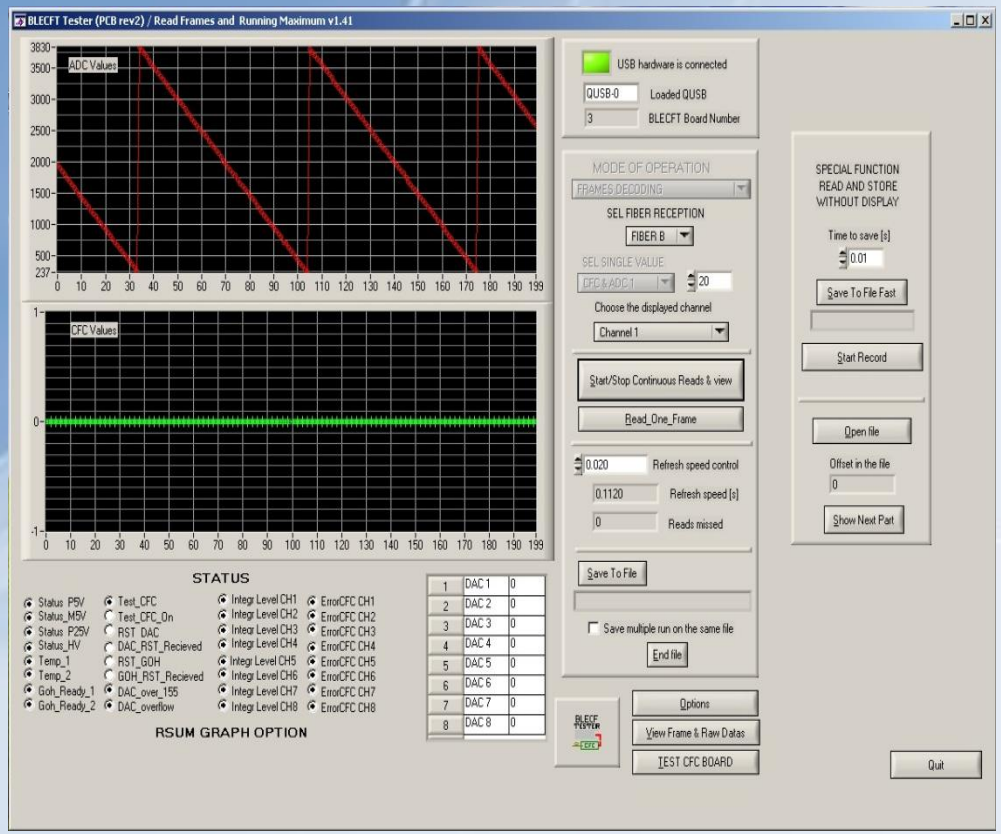
BLECF software presentation

- Developed in C with Labwindows/CVI (NI)
- Can read and decode the frames send from the BLECF at 100Hz, show it and save it inside a file.
- Can show and save the result of the BLM processing which is inside the BLETC.
- On top of this, the test mode can make the functional test of the BLECF.

BLECF software presentation

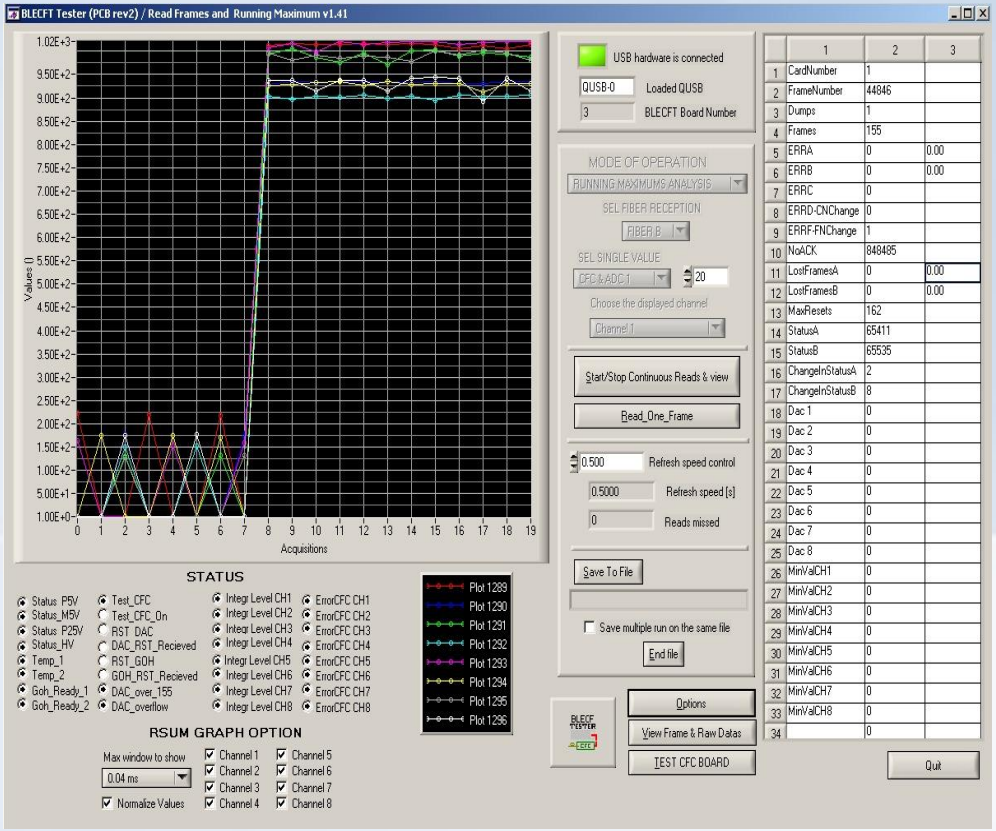
Frame mode

The software takes the complete frames from the BLECF , analyze it and show it.



Running sums mode

The core processing of the BLM system holds inside the FPGA taken from the BLETC. The software takes the result of it and show it.



BLECF functional test

1. 10pA calibration
   Look at the ADC readings
   Calculate the exact current
   The operator correct it on the board
   Check if there are discontinuity
   Check if the signal is saturated
   Save the final value inside a file

2. 1mA calibration
   Done with a external current source (keithley)
   The operator correct it on the board
   Save the final value inside a file

3. Complete test
   Check the integrity of the optical fiber link
   Check if the status are working
   Check the HV level thresholds
   Check the linearity with internal sources
   Save everything inside a file

REPORT_CFCBoard_NormalT__DN_67_0.txt - Notepad

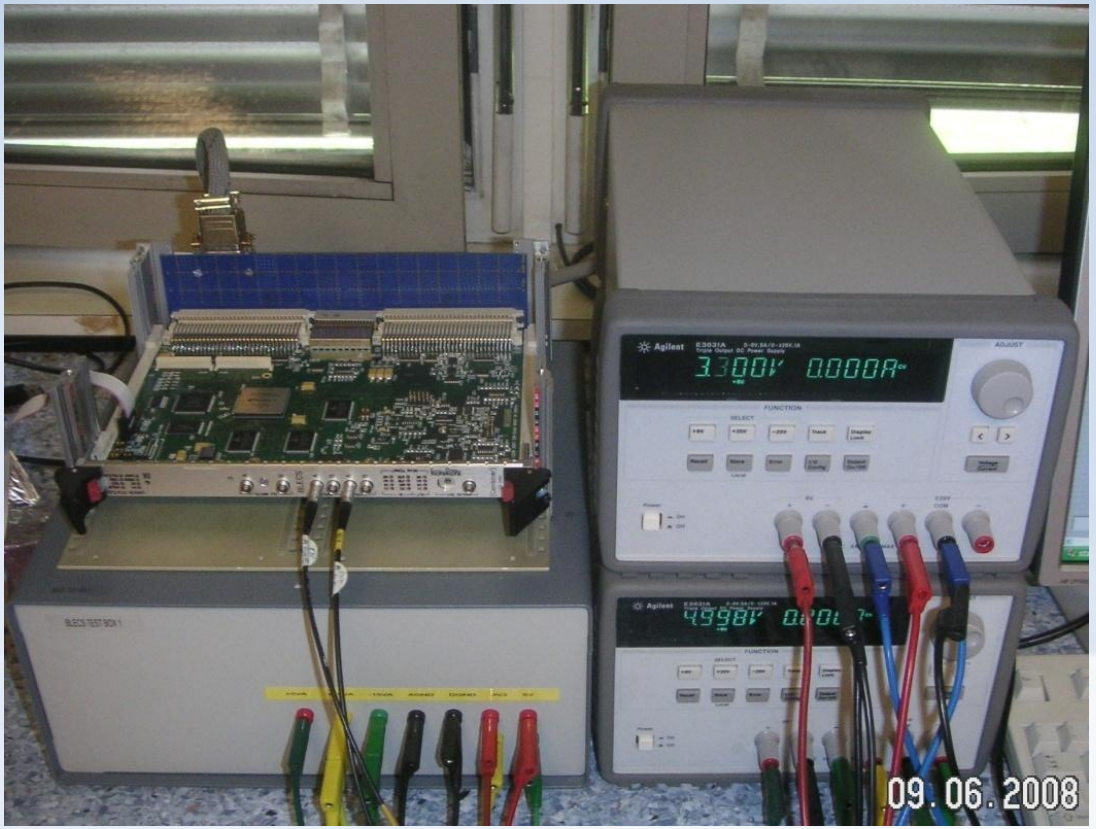
File Edit Format View Help

```
G:\\Divisions\\sl\\DIV_SL\\BI\\PM\\BLM_BLECF\\BLECF_TEST_REPORT\\REPORT_CFCBoar

FUNCTIONAL TEST OF THE TUNNEL ACQUISITION BOARD FOR THE LHC

Mon Oct 15 14:10:53 2007

------------------------------------------------------------

Device number send through the fiber : 67

PCB version : EDA-00593-V6

Comments :
Type your comments that will appear in the report file

------------------------------------------------------------

IDENTIFICATION BARCODES
------------------------------------------------------------
-- DONE -- (FPGA barcode number, FPGA internal number, Board number)    passed
------------------------------------------------------------
BLECF_0067
FPGA  N0.067
- 0006222348proto005
30201010069242
30201010056165


MEASURE 10PA => Start at 256908.18 [s]  (12.50 - 25.00)
------------------------------------------------------------
CALIBRATION Offset current CH1 : 19.66 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH2 : 18.97 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH3 : 19.78 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH4 : 19.66 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH5 : 20.67 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH6 : 19.58 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH7 : 19.23 [s]    (12.50 - 25.00)           passed
CALIBRATION Offset current CH8 : 17.98 [s]    (12.50 - 25.00)           passed
Offset current calc CH1 : 10.17 [pA]    (16.00 - 8.00)                  passed
Offset current calc CH2 : 10.55 [pA]    (16.00 - 8.00)                  passed
Offset current calc CH3 : 10.11 [pA]    (16.00 - 8.00)                  passed
Offset current calc CH4 : 10.17 [pA]    (16.00 - 8.00)                  passed
Offset current calc CH5 : 9.68 [pA]    (16.00 - 8.00)                   passed
Offset current calc CH6 : 10.22 [pA]    (16.00 - 8.00)                  passed
Offset current calc CH7 : 10.40 [pA]    (16.00 - 8.00)                  passed
Offset current calc CH8 : 11.12 [pA]    (16.00 - 8.00)                  passed
Overshot      CH1 : 0    (Max 20)                                       passed
Overshot      CH2 : 0    (Max 20)                                       passed
Overshot      CH3 : 0    (Max 20)                                       passed
Overshot      CH4 : 0    (Max 20)                                       passed
```

BLECS test bench

Test bench 1

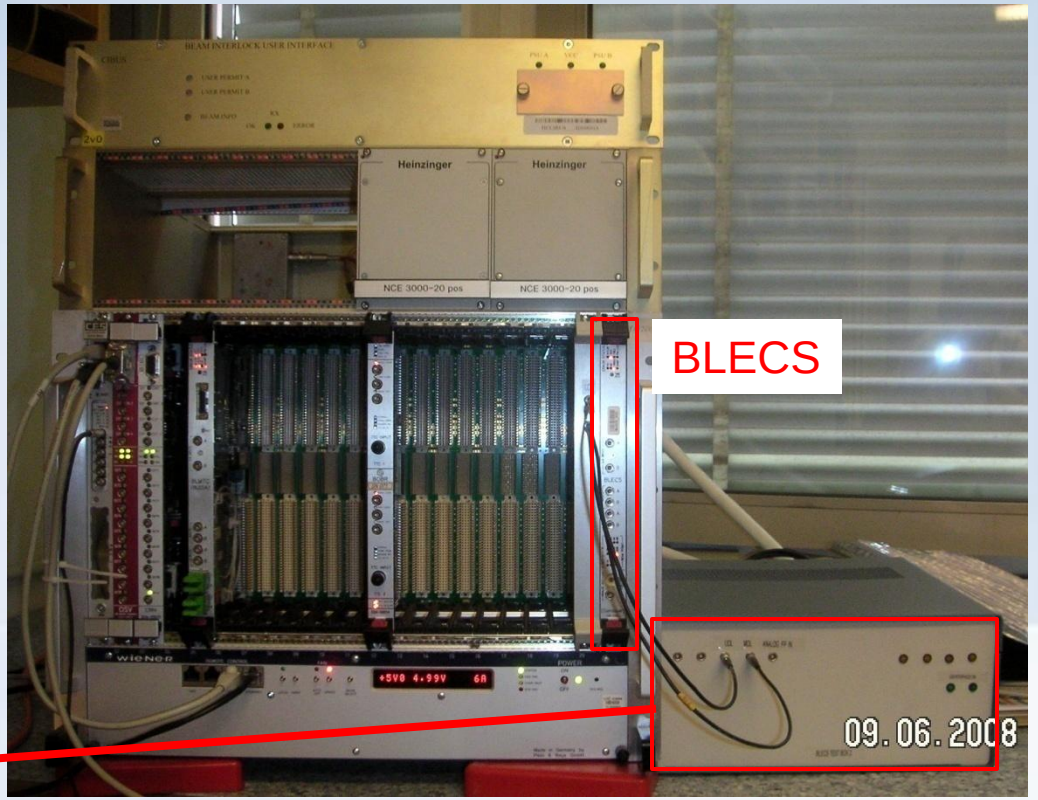
- Current measurements at all programming stages
- Automation of the 2 PS with Labview: lowering each voltages, look at the status when it changes (comparators thresholds check) and save the result inside a file



BLECS test bench

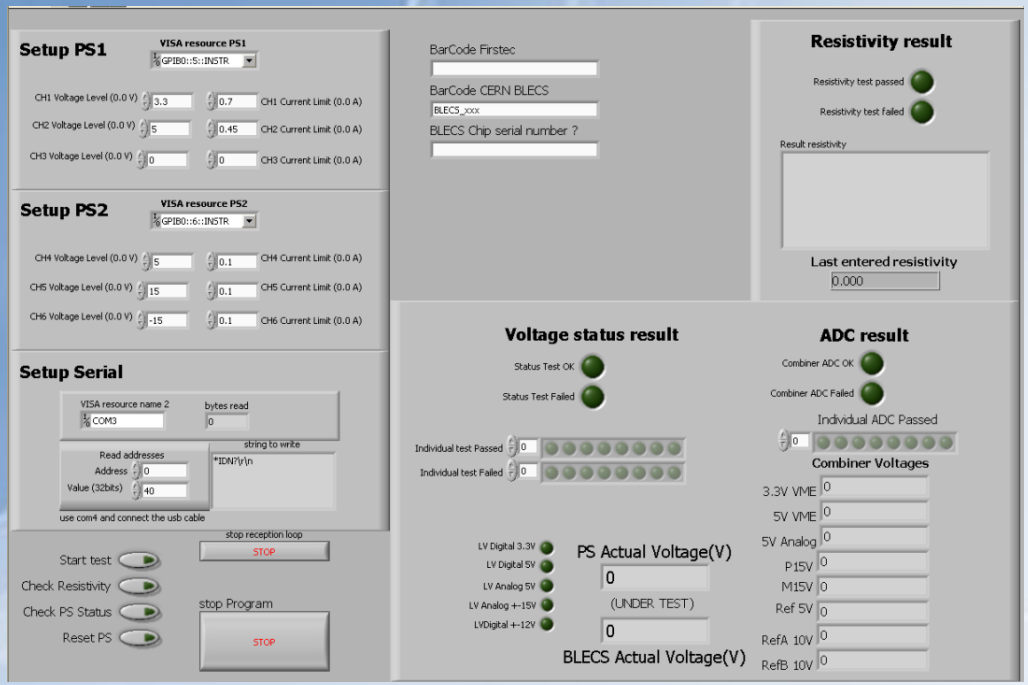
Test bench 2

- Use a standard BLM LHC crate
- Use 2 I/O modules from NI to drive the BLECS inputs and check the outputs.
- Gets data from the BLECS with the CMW wrapper (AB-CO-MA)

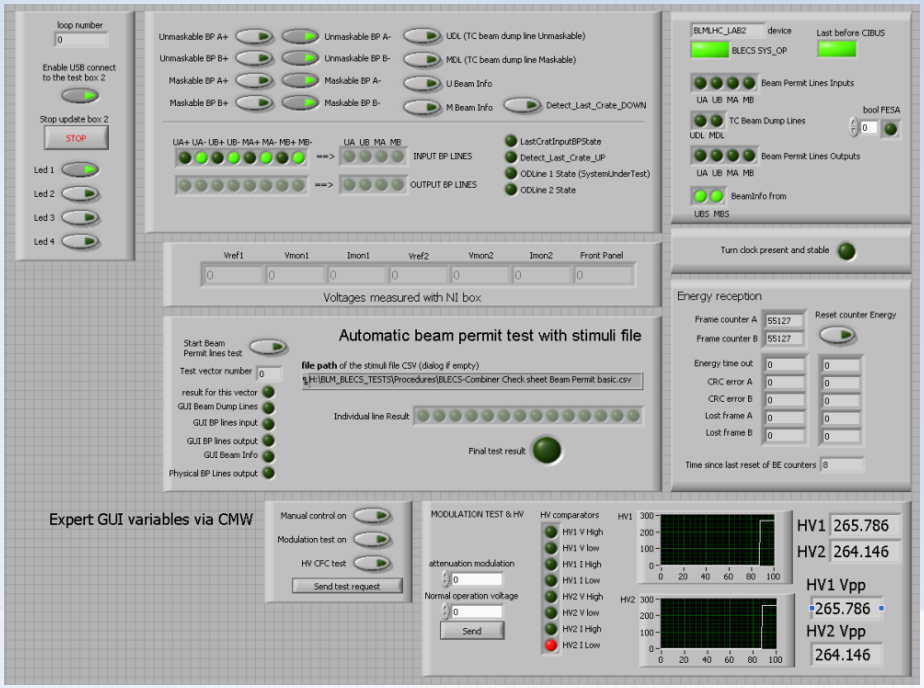


BLECS test bench

Test bench 1



Test bench 2



Summary

BLECF test bench

- Aim to be used to test 750 boards in the lab and in the tunnel
- Ability to test FPGA code
- Custom test board using commercial modules
- Software in Labwindows/CVI
- Calibration assistance
- Full automated functional test
- Saves full measurement into multiples files

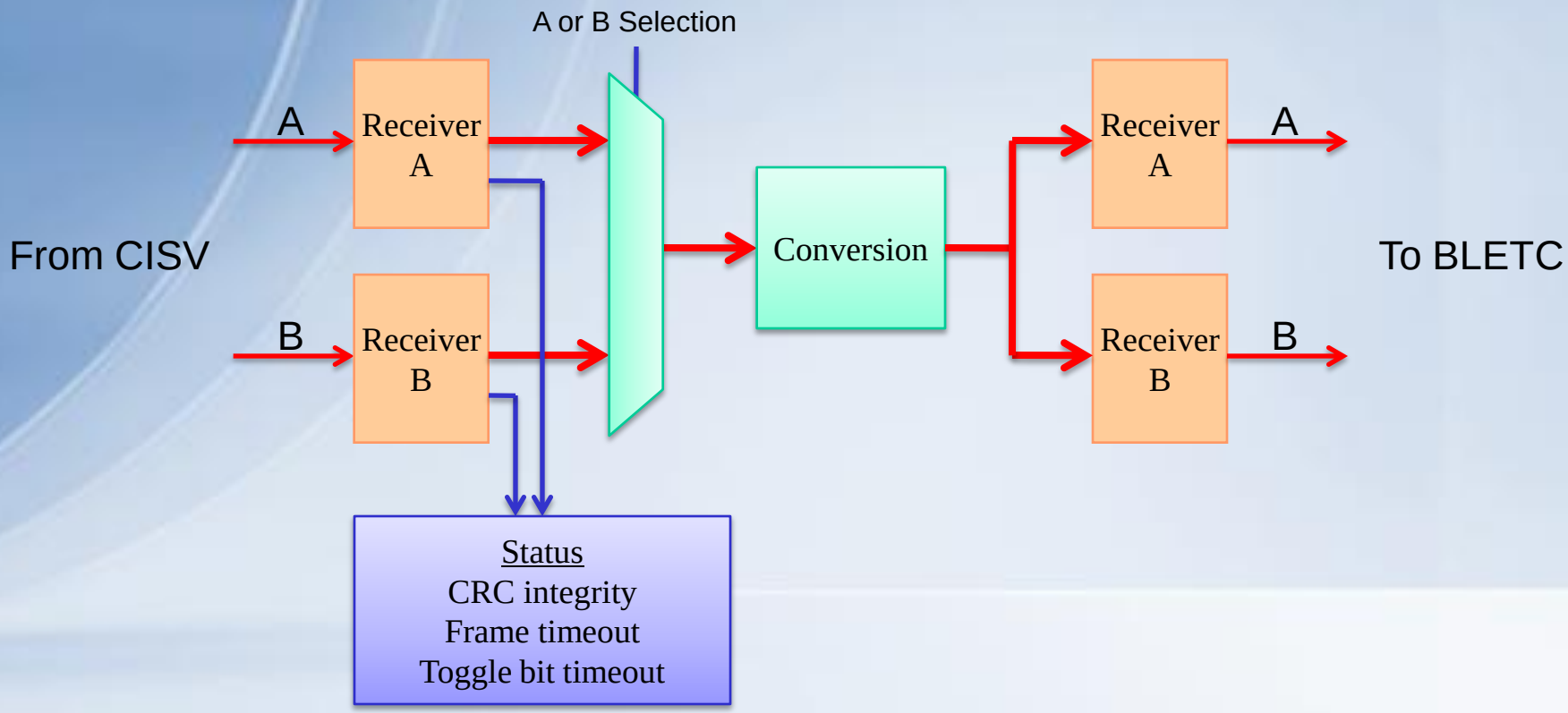
BLECS test bench

- Aim to test 45 boards
- Ability to test FPGA code
- Use commercial input/outputs modules (analog and digital)
- Software in Labview
- Partial automation for complex logic (all beam permit lines states)
- Uses status of the FPGA continuous check for the energy reception, turn clock.
- Test report on a excel file

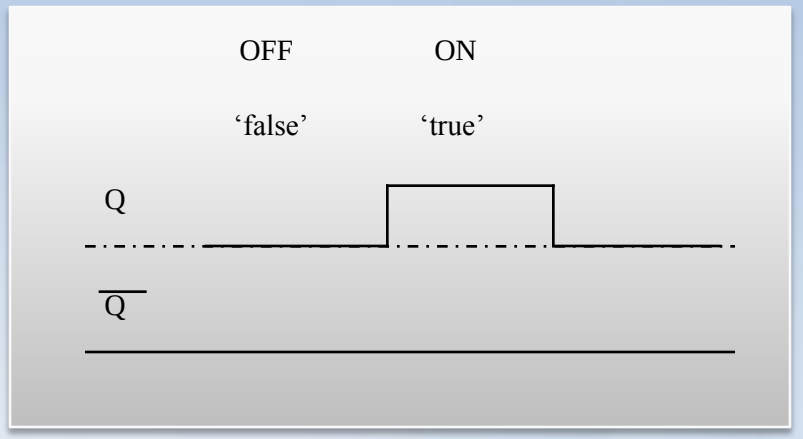
Audit of the BLM LHC system

Additional slides

Beam energy conversion

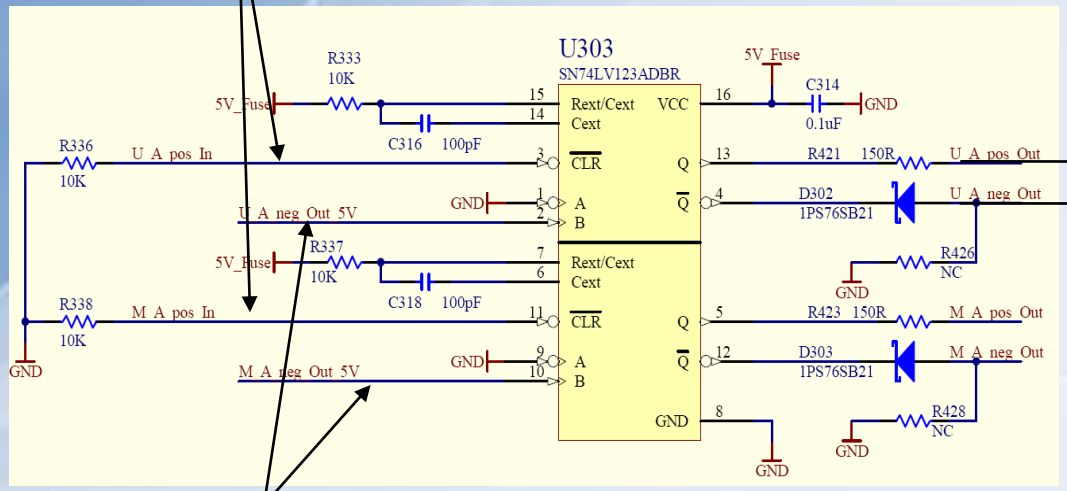


Beam permit

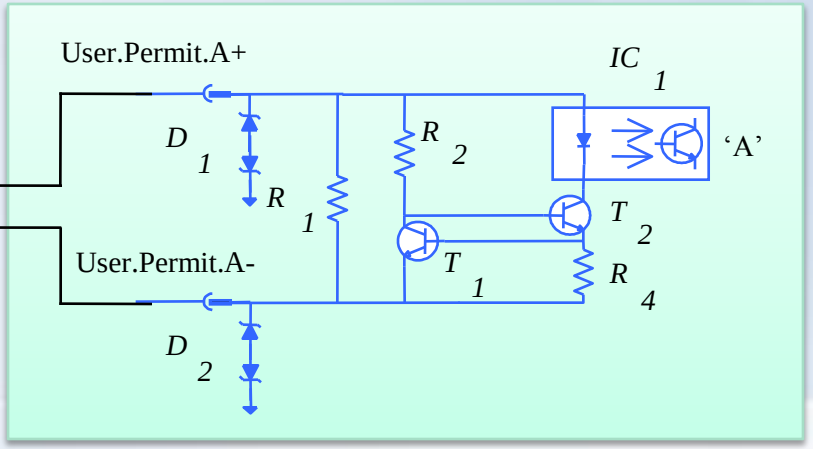


Lines from BLECS (Up)

Combiner outputs



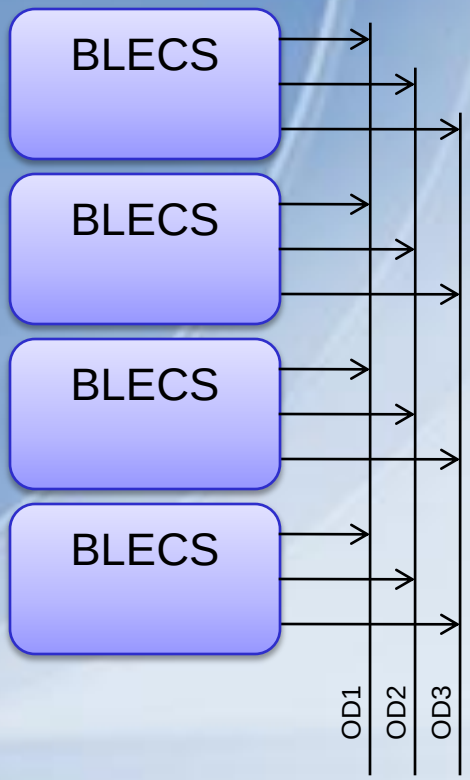
CIBUS interface



Lines from FPGA (frequency > 1MHz)

http://ab-div-bdi-bl-blm.web.cern.ch/ab-div-bdi-bl-blm/Electronics/BLECS_Combiner/BLECS-Schematics/Rev3/BLECS_Combiner_Rev3.pdf

Commune lines between crate



Signalization needed:

1) The system is under test
   (the last crate keep the beam permit lines low)
2) The last crate has received the beam permit low
   (See *BPTC test)*
3) *Request 100pA test level*
4) *Request "Modulation level " of the HV+ Modulation of the HV*

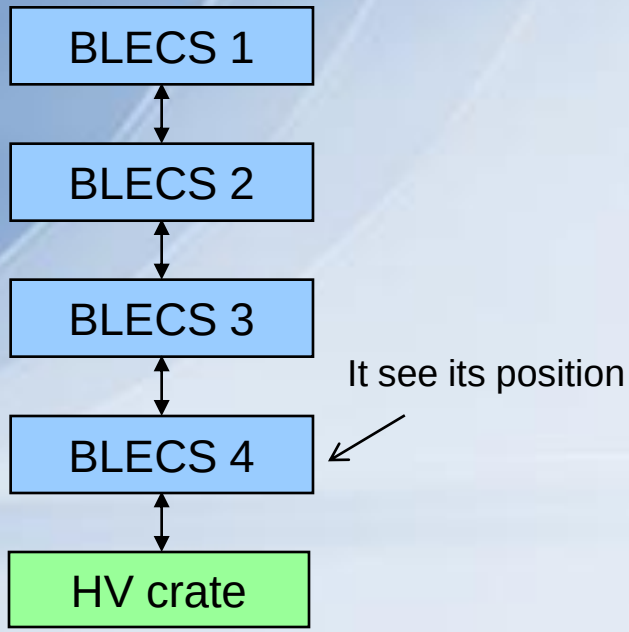
Name	OD1	OD2	OD3	Description
Normal operation	1	1	1	
Beam permit indication from the la combiner before the CIBUS	x	x	0	OD3 can change to indicate BP is false by the last crate before CIBUS (See BPTC test)
System under test (all test except Modulation)	0	1	x	The HV level goes at 100pA when any test starts
System under test Request Modulation level and Modulation.	0	0	x	

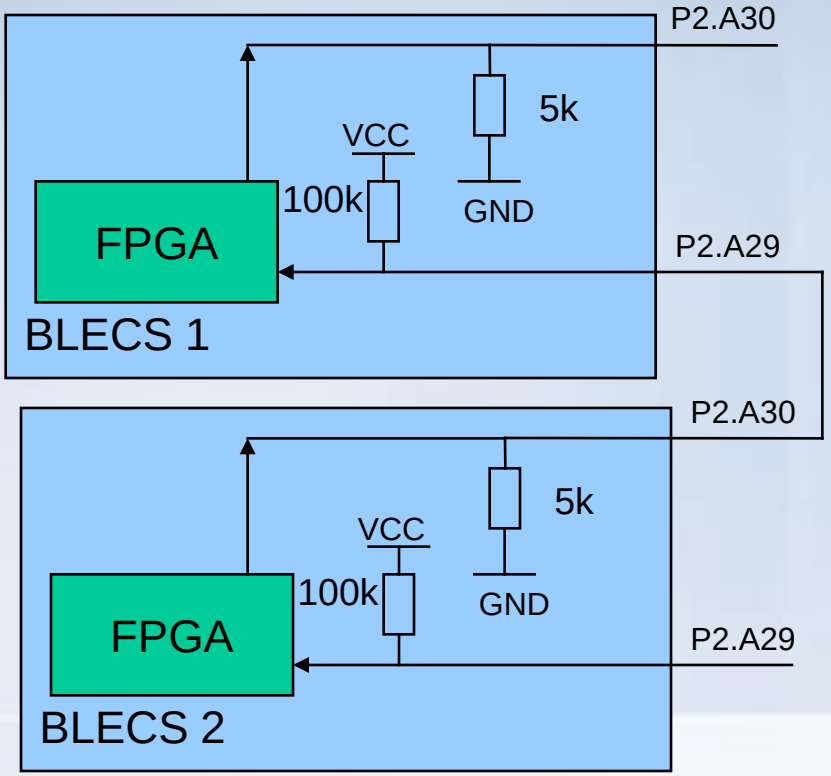
Open drain lines with dedicated IC: OD1 & OD2

Line direct FPGA to FPGA (200 Ohm between IO) simulation of OD with pull-up OD3

Last crate identification

Task :
Identify the last crate in the chain
(the one which is connected to the CIBU)

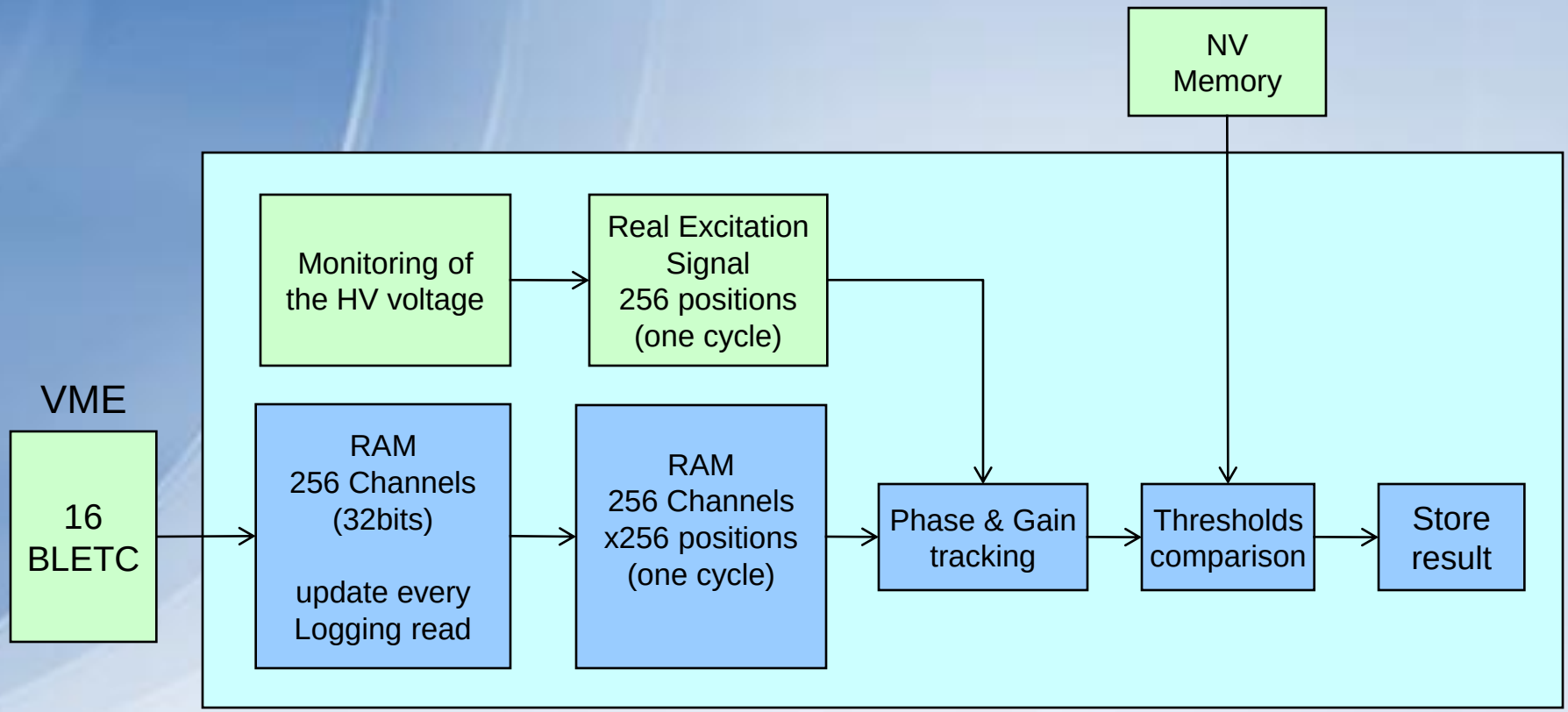




If the FPGA input = '0' there is another BLECS under. Means this is not the last BLECS before CIBU.

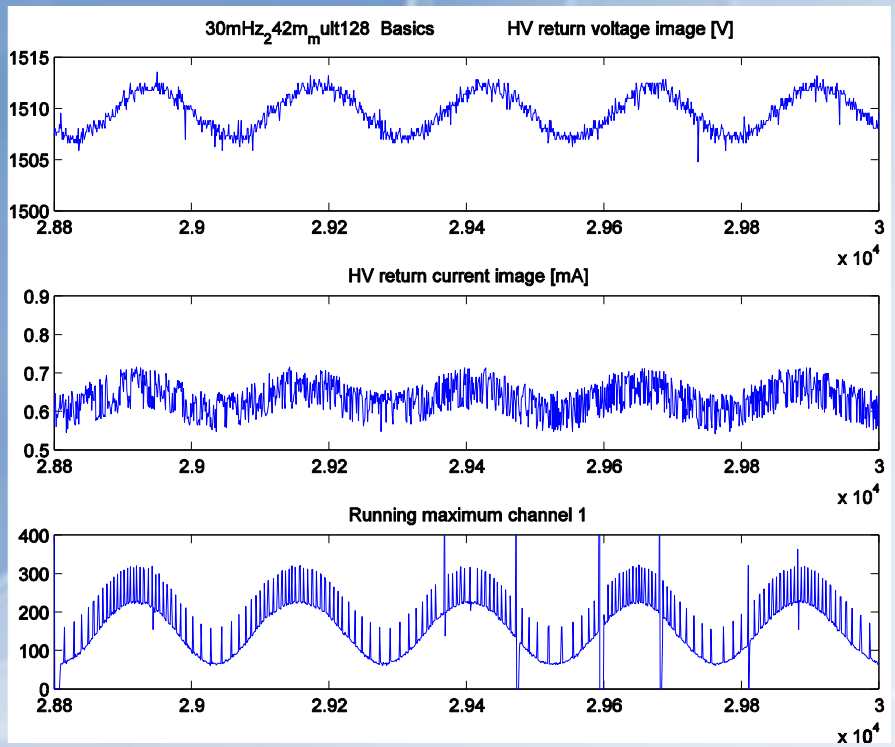
If the FPGA input = '1' there is no BLECS under. Means there is the CIBU and this is the last BLECS before CIBU.

Tests: HVLF (HV modulation)



Excitation Signal frequency 30mHz or 100mHz
Sample per period 256 for the reference and 1Hz samples for the Running maximums (Use the Login)
The processing is done sequentially for each channel

HVLF first results (2007)



There are only 4 channels connected with a chamber for this test. There can be easily identified them on the result of the measurements below.

30mHz 242m

immediate =

9.1940	0.4452	226.5720	36.6587
9.1599	0.4314	228.4305	13.0265
9.3847	0.5069	178.9234	95.3153
8.9925	0.2060	231.5079	13.3753
0.1682	0.3742	78.4421	46.1785
0.6278	0.7993	27.9301	21.5241
0.4022	0.4905	86.9017	66.4131
0.6178	0.8284	118.8510	94.8222

DoubleCorr =

41.9108	0.6179	-20.4725	3.9340
43.3491	0.4041	-18.6534	0.4829
42.4540	1.3481	-22.7531	3.2956
43.4921	16.5967	-23.1285	8.9557
4.0004	28.2424	-120.5595	113.6085
2.6916	24.2729	57.1366	43.3929
6.2551	34.6915	21.2913	100.1327
11.3780	49.7038	81.2672	35.3149

100mHz 242m

immediate =

12.1107	1.0248	173.3955	7.1126
12.3805	1.1027	173.6836	6.7431
12.0633	0.9386	174.3464	6.7139
13.1374	4.4002	174.1024	6.6918
21.2848	54.7866	182.5379	23.5718
2.7935	2.7699	120.6894	59.7021
22.3639	58.5646	173.3897	14.2236
2.2831	2.3579	157.5595	19.3444

DoubleCorr =

53.9235	0.3861	-74.4530	1.5469
53.8760	0.4452	-73.0477	0.5569
52.8174	0.9205	-77.1295	1.1664
52.6185	9.6636	-76.7563	9.3191
5.6117	29.1210	-17.5239	113.2888
4.2740	27.1789	38.5408	134.2654
4.4643	25.2598	-4.0951	123.3614
8.6702	40.6656	64.9081	42.5117

Gain StdDev Phase StdDev

In this test, there were two methods working in parallel: Simple and double cross-correlation
Further investigations needed to ameliorate, select one of the two and fine pitch the method.