EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN – AB DEPARTMENT

BLM acquisition chain self-test functionalities

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Abstract

Achieved during technical student period May 2006 - May 2007
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The LHC beam loss monitoring system is aimed to protect the collider against damage due to wandering particles, by giving a beam dump signal if their number reaches a given threshold. This system relies on a complex acquisition chain, which state must be periodically tested to ensure proper operation and measurements accuracy. The purpose of this document is to give details on this self-test functionalities implemented beside the BLM electronics.

Geneva, Switzerland
May 14, 2007

Contents

1 Instant value test

1.1 General

The instant value test gives an information about the instant status of the BLM acquisition chain. It's purpose is to test the global functioning of the chain before the start of each new LHC cycle. In the case of an important failure detection (cable broken, short circuit, ...) a *Status* signal will inform the operators that the BLM system is out of order, and additionally the location of the problem.

The self-test is located in the BLECS (combiner card) and should perform its test on the data provided by the logging given by 16 BLMTC cards. Please report to *Christos Zamantzas* for more information on the BLMTC data logging. Because each BLMTC handles 16 acquisition channels, the self-test functionalities should perform their processing on 256 channels within a given delay.

The chosen method is an harmonic analysis of the chain.

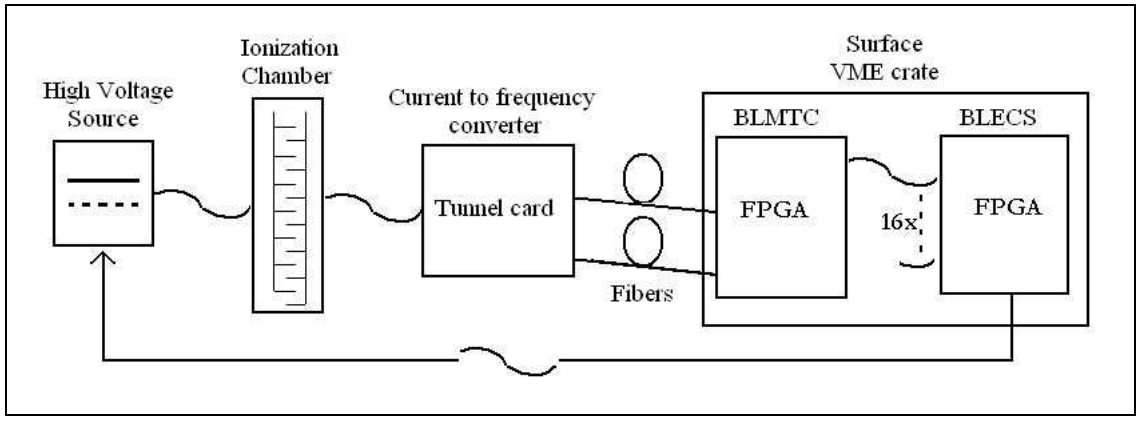

Figure 1.1: *Composition of one BLM acquisition channel*

A little modulation signal is generated on top of the high voltage source command input. The response of the system is given by comparing this reference signal with the output given at the end of the chain.

For the instant value test, a single cross correlation is used to give representative (but not exact) values of the gain and the phase. These values can be compared at each run of the test to a range of initial values given at LHC startup. Because of the effort made to reduce the sensitivity in order to be able to detect general failures, this block should not be able to measure aging factors of the chain. The second part of this documents is giving details on the long term analysis function, providing that specific information.

1.2 Features

This block is designed as an add-on to the combiner design.

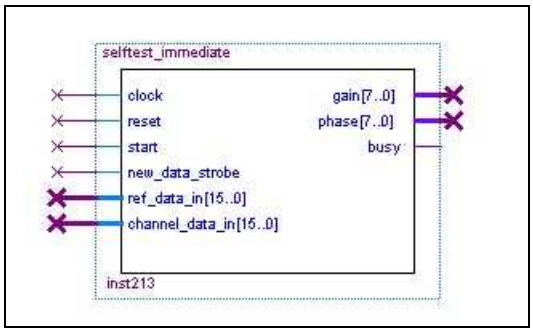

Figure 1.2: *Instant value self-test block*

The system is designed around a single convolution function and a Moore-type finite state machine. One clock is distributed in the block, and should be the 1 MHz clock available in the host design. The input signals on which is processed the calculation are the reference (stimulus) signal and the chain output (running sums logging) data. Both are 16 bit wide inputs, but to reduce unneeded register generation at synthesis time, the offset (some MSB's) can be forced low. This reduces the amount of logic generated without loosing in precision.

Additionally, both inputs are filtered by the same second order Butterworth filter, so both inputs can be noisy. This is in particular the case if the reference signal is connected to the high voltage source feedback monitor. In this case, the analysis is performed only on the section of acquisition chain composed by the ionization chamber, the CFC electronics, and the running sums.

The output values are : an **indication** on the gain, and a phase value, both 7 bits wide. Because the processing is done on 256 samples (representing 360 degrees), the given phase value must be multiplied by $360/256$ to obtain a value in degrees. The block has been tested in difference conditions, and the sensitivity is tuned to give stable values if the basic working conditions of the chain are met.i

One test cycle is made of an acquisition phase, and a processing phase. The acquisition phase is turned on by a high level on *start* input and is lasting the time of one signal period, acquiring thus always 256 samples of both the running sums signal and the reference. Trigger of value acquisition (ie. signal *newi_data_strobe*) must correspond to the presence of a new sine value available out of the modulation generator. The processing phase is lasting $256 * 256$ clock cycles, because of the complete moving window correlation operation implemented between two 256 samples of each signal.

Please take note that due to the presence of two infinite impulse response filters, there is a settling time of two periods before a measurement is accurate. After the processing a *busy* signal is put low, telling a global combiner control unit (to be created) that the test on one cycle is finished. Do not attempt to read the output values before this signal is low.

1.3 Implementation

Here is the block diagram of the instant value self-test without the control unit, to explain the processing principle.

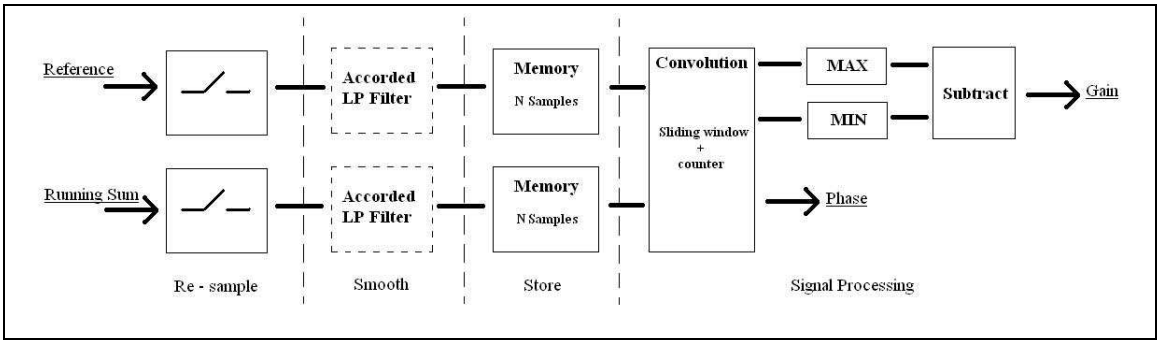

Figure 1.3: *Instant value self-test principle*

During the acquisition phase, the two RAM blocks are filled up with 256 samples of the reference signal and the running sum signal output by the filters. Here the control unit counts 256 new sine wave values to know when to enter in the processing mode. Both RAM blocks are inferred automatically during synthesis by the Altera Quartus © compiler tool. The filters a second order Butterworth-like infinite impulse response filters, with 16 bit long fixed point coefficients and registers. Because we are always working on 256 samples signals, is was possible to fix the cut-off frequency to the double of the input frequency.

Filter Equation :

$$H(z) = \frac{z^{-2} + 2.z^{-1} + 1}{b_1.z^{-2} + b_2.z^{-1} + C}$$

with

$$b_1 = \left(\frac{2}{T_s.\omega_c}\right)^2 - \frac{2.\sqrt{2}}{T_s.\omega_c} + 1 \qquad b_2 = -\left(\frac{2.\sqrt{2}}{T_s.\omega_c}\right)^2 + 2 \qquad C = \left(\frac{2}{T_s.\omega_c}\right)^2 + \frac{2.\sqrt{2}}{T_s.\omega_c} + 1$$

Sampling rate is $T_s = \frac{1}{F_s} = \frac{1}{256.F_{in}}$ (256 sample per period)

and cut-off frequency is $\omega_c = 2\pi.F_c = 2\pi.2.F_{in}$

$\Longrightarrow$

$$T_s\omega_c = \frac{2\pi.2i.F_{in}}{256.F_{in}} = \frac{4\pi}{256}$$

The convolution block is based on a MAC (Multiply-Accumulate) primitive, also directly inferred by the synthesis tool. It performs a complete circular moving window correlation between the two signals. The reference is sliding on the running sum signal to be able to detect a max peak when both are in phase. At this the number of iteration counts gives the phase between the 2 signals.

The information on the gain is given by the difference (implemented with a combinatory subtractor) of the highest value and the lowest value of the correlation result.

2 Long term analysis

2.1 General

The aim of this functionality is to perform a long term analysis on the acquisition chain, to see the impact on the accuracy over a long time. This can vary due to the radiation and global aging of the electronics. The analysis is here done on the whole acquisition chain, including the high voltage source the running sum operation and the filter.

The principle of this transfer function analyser is described in *C.S. Elsden and A.J. Ley , A digital transfer function analyser based on pulse rate techniques. In: Automatica, IFAC Vol. 5, Elsevier, Amsterdam (1969), pp. 51.60.* It is based on two concurrent cross correlation operations, with 2 ideal references, from which we know all the characteristics. The input signal for the Block Under Test is the output of the running sums.

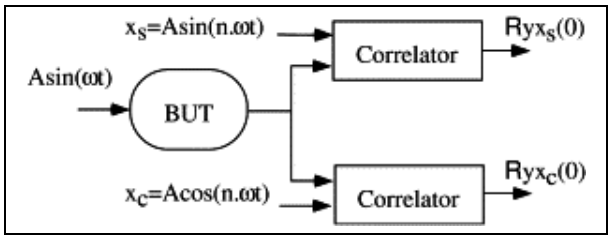

Figure 2.1: *Long term analysis principle*

The gain and the phase are giving by :

$$|H| = \frac{1}{A^2} \cdot \sqrt{\Re_{yx_{cos}}{}^2 + \Re_{yx_{sin}}{}^2}$$

$$\Phi(H) = \arctan\left(\frac{\Re_{yx_{cos}}}{\Re_{yx_{sin}}}\right)$$

2.2 Features

Here again, the block is designed to be simply dropped anywhere in the host design. Here is a representation of the block :

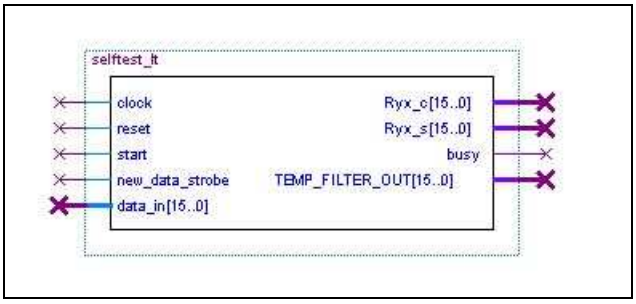

Figure 2.2: *Long term self-test block*

The same 1 MHz clock is used as the instant value self-test, and reset signal is active low. There is one single input retreiving data from the running sums. The two ROM's are included

in the block and have an amplitude (A) of 128, signed two's complement in the negative part.

To be accurate, the *start* signal must trigger the beginning when the stimulating sine signal is at the origini, and after a few periods of filter registers filling. This means that a *begin_of_period* signal should exist in the modulation generator connected to the long term self-test.

The outputs are the result of the two cross correlation operations, given in signed two's complement representation, on 16 bits. The processing of the gain and the phase should be done in an remote computer, with plotting capabilities to see the evolution of the chain at long term.

2.3 Implementation

Concerning the implementation of the block, here is a simple block diagram, again without the main control unit :

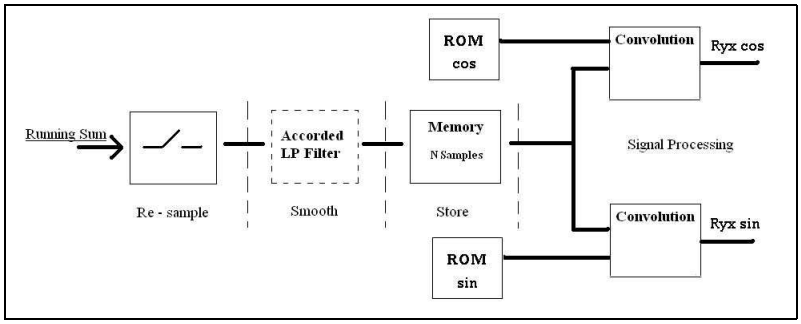

Figure 2.3: *Long term analysis implementation*

Here again, a filter is present to smooth the running sum signal, and is included in the analysis path. Additionnaly the correlation operation is not a complete sliding window correlation, but a single MAC (Multiply ACcumulate) on a whole period, at offset zero. This explains why the synchonization of the start signal with a period start is such important.

The processing of the data is done in signed arithmetic, and should not be influenced by an offset of the running sum data. However, to prevent the synthesis tool to infer large amounts of registers for signal processing part of the device, a previous study must be done on the signals. For examples, removing too large offset (typically present in running sum data) by pulling low some MSB's should avoid the design space to explode, and also result in a gain of precision. Tests has been made on Running Sum number 7 (which sould be choosen for it's good characteristics) and only 10 relevant bits where needed to the systeme to be optimally accurate.