Critical signal path inside the BLECS Combiner card (23.11.2010)

The beam permit signals Unmaskable and Maskable from the BLETC to BLECS are transiting through the backplane of the crate on the P0 connector (the one in the center of the card)

VME BI backplane specification: https://edms.cern.ch/file/365170/1/VME.Spec.365170.pdf
Or http://ab-div-bdi-bl-blm.web.cern.ch/ab-div-bdi-bl-blm/Electronics/crate_wiener/VME.Spec.365170.pdf

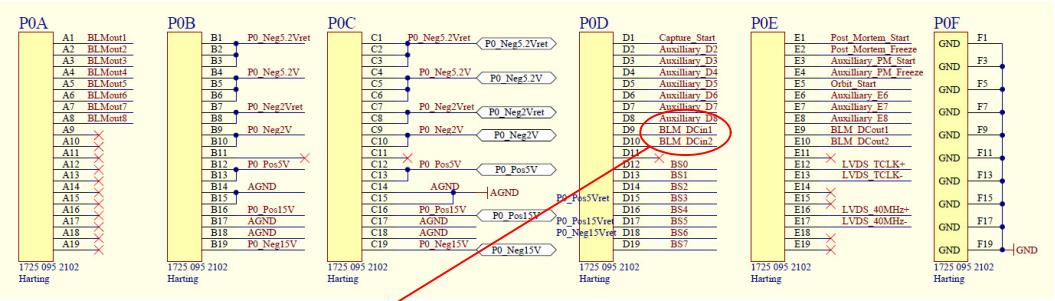
Daisy chain1-1 (9 d and e) = Unmaskable
Daisy chain1-2 (10 d and e) = Maskable

Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	Bus line-0	-5V2RET	-5V2RET	HW Low Byte 1 bit 0	HW High Byte 1 bit 0	GND
2	GND	Bus line-1	-5V2RET	-5V2RET	HW Low Byte 1 bit 1	HW High Byte 1 bit 1	GND
3	GND	Bus line-2	-5V2RET	-5V2RET	HW Low Byte 1 bit 2	HW High Byte 1 bit 2	GND
4	GND	Bus line-3	-5V2	-5V2	HW Low Byte 1 bit 3	HW High Byte 1 bit 3	GND
5	GND	Bus line-4	-5V2	-5V2	HW Low Byte 1 bit 4	HW High Byte 1 bit 4	GND
6	GND	Bus line-5	-5V2	-5V2	HW Low Byte 1 bit 5	HW High Byte 1 bit 5	GND
7	GND	Bus line-6	-2VRET	-2VRET	HW Low Byte 1 bit 6	HW High Byte 1 bit 6	GND
8	GND	Bus line-7	-2VRET	-2VRET	HW Low Byte 1 bit 7	HW High Byte 1 bit 7	GND
9	GND	GPPL-0	-2V	-2V	Daisy chain1- 1-in	Daisy chain1-1-out	GND
10	GND	GPPL-1	-2V	-2V	Daisy chain 1-2-in	Daisy chain 1-2-out	GND
11	GND	GPPL-2	GPPL-3	GPPL-4	GPPL-5	GPPL-6	GND
12	GND	Bus line1-0	+5V	+5V	Bunch Select 1 Bit 0	LVDS Turn clock Delay 1 +	GND
13	GND	Bus line1-1	+5V	+5V	Bunch Select 1 Bit 1	LVDS Turn clock Delay 1 -	GND
14	GND	Bus line1-2	+5VRET	+5VRET	Bunch Select 1 Bit 2	TTL Turn clock Delay 1 +	GND
15	GND	Bus line1-3	+5VRET	+5VRET	Bunch Select 1 Bit 3	TTL Turn clock Delay 1 -	GND
16	GND	Bus line1-4	+15V	+15V	Bunch Select 1 Bit 4	LVDS 40 MHz Clock 1 +	GND
17	GND	Bus line1-5	+15VRET	+15VRET	Bunch Select 1 Bit 5	LVDS 40 MHz Clock 1 -	GND
18	GND	Bus line1-6	-15VRET	-15VRET	Bunch Select 1 Bit 6	TTL 40 MHz Clock 1 +	GND
19	GND	Bus line1-7	-15V	-15V	Bunch Select 1 Bit 7	TTL 40 MHz Clock 1 -	GND

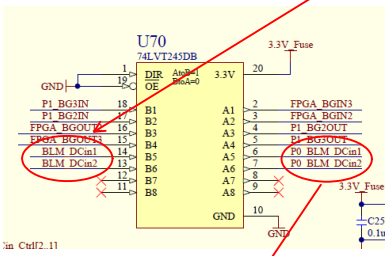
Table 6a: Pin allocations on J0 for slots 3 to 11 (Front view)

This daisy chaining of the BLETC are ending at the last position in the crate (Slot 21) where the combiner is installed.

Combiner hardware schematic: https://edms.cern.ch/file/887601/1/EDA-01660-V3-0_sch.pdf
Or http://ab-div-bdi-bl-blm.web.cern.ch/ab-div-bdi-bl-blm/Electronics/BLECS_Combiner/BLECS-Schematics/Rev3/BLECS_Combiner_Rev3.pdf

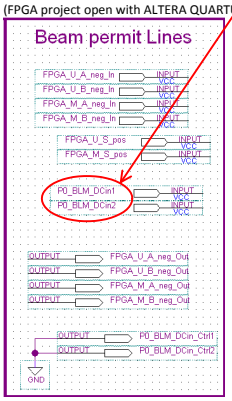


Then they passing through a buffer:



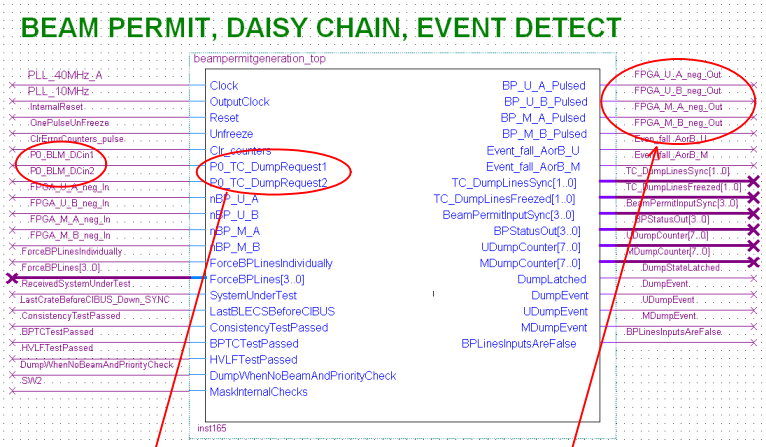
To arrive inside the FPGA:

(FPGA project open with ALTERA QUARTUS)

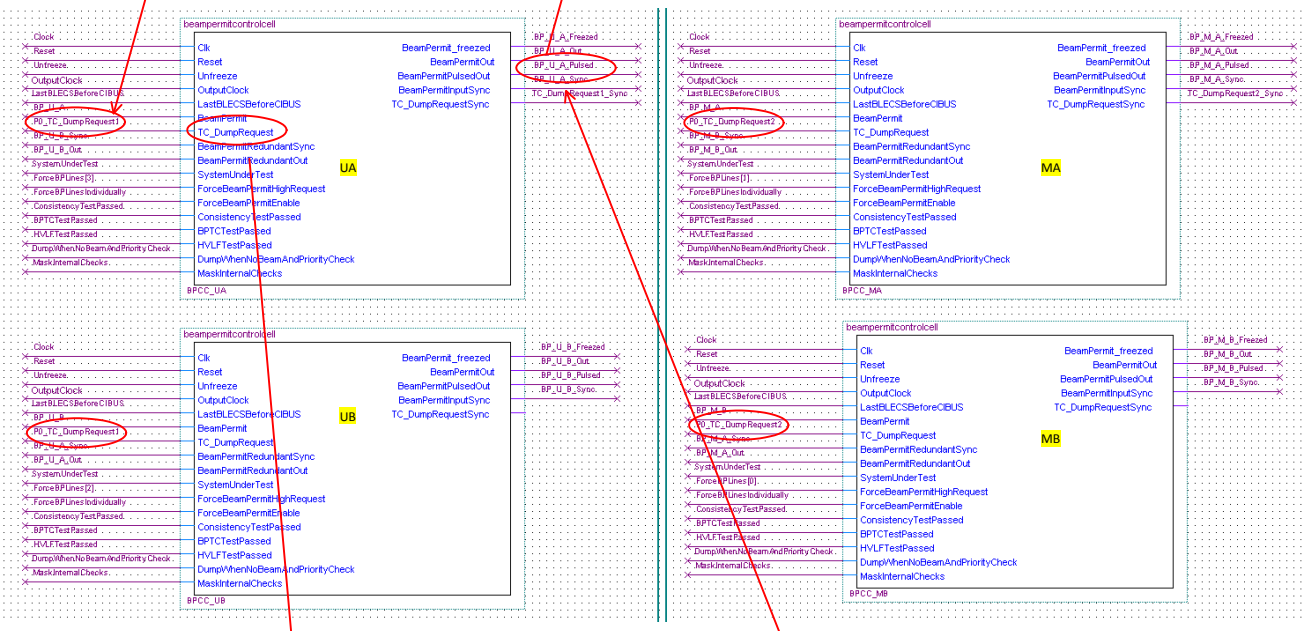


We can see also the inputs from the crates (FPGA_x_x_neg_In) for Unmaskable (U) and Maskable (M) with redundancy (A and B)
The outputs going to the BIS interface (or another crate) can also be seen (FPGA_x_x_neg_Out)

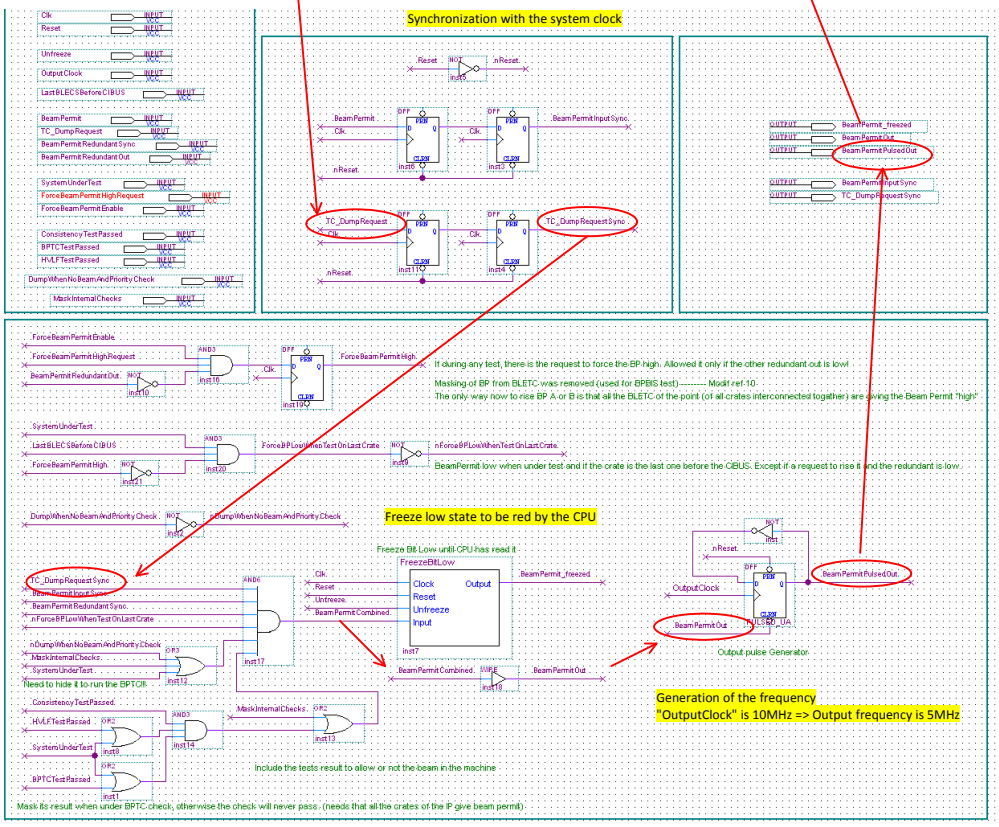
(Next page) From the Top Schematic entry of the FPGA project: The beam permit lines are going directly to the block "BeamPermitGeneration_top"



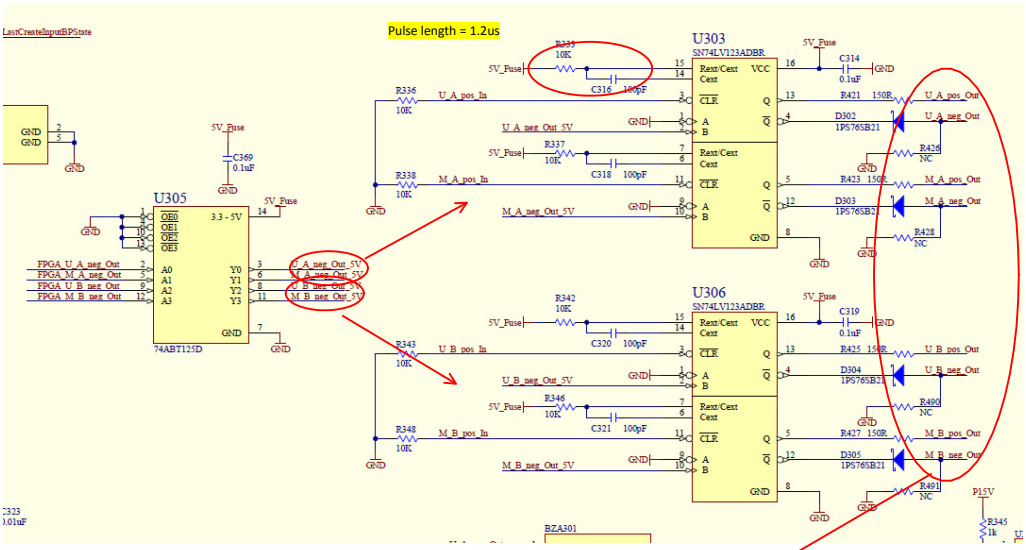
Inside this block, each "BeamPermitControlCell" is assigned to take care of one signal (U or M and A or B). The signal from the BLETC is splited at this level between the redundant block A and B



Inside each of the block the combination is done:
After being synchronized, the beam permit signal from the BLETC (TC_DumpRequest) is combined with other signal (including the signal from other crates "BeamPermit") to generate
The final signal "BeamPermitCombined" . This signal controls the generation of the frequency. This frequency leaves the FPGA.



Ones the 4 signals are leaving the FPGA, they go to the retriggerable one-shot circuit (SN74LV123):
In order to give a "High" at its outputs Q (pin 13 and 5), a frequency higher than the pulse length (1.2us) must be present at the clocks inputs "B" (pins 2 and 10).
At this level, you can also see that there is a (second time) combination with signals from other crate (x_x_pos_In) through the !CLR input (Propagation of beam permit signal without passing through the FPGA)



The output lines (positive and negative, U and M, A and B) are then routed to the connector P2 user assignable lines (free lines specified in the VME64 standard).
There are a transition card (no electronic on it) behind the VME crate where cables are connected to make the links between the crates and to the BIS interface (CIBUS).