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Details and specifications of the beam energy transmission in the BLM electronics

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Abstract

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To keep the BLM electronics accurate during the whole beam lifetime, the threshold values should continuously be adjusted with the value of the beam energy. This paper describes the beam energy data path through the BLM electronics, and gives the details on the implementation of the serial links needed to keep the threshold values always updated.

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Contents

1 Introduction

The beam loss section's mandate is to measure, process and interpret instant beam losses, to trigger beam dumps whenever it can become dangerous or incontrollable. Because of the never reached energy levels the LHC is foreseen to explore, a significant effort is made to ensure the reliability and accuracy of the the BLM electronics.

During a beam lifetime of 10 hours, the energy contained in the ring will be varying, depending if the LHC is in injection, accelerating or colliding phase. To ensure the accurate adjustment of the beam dump threshold values during these phases, a beam energy measurement (called BEM in this document) value should be provided to the BLM electronics. This measurement exists and is provided to the whole equipment along the tunnel by the AB-BT group. But the distribution and use of this beam energy measurement is ours to implement. This document handles about this issue, giving further details on BLM specific and failsafe considerations.

The aim of this document is to provide useful information to enable easy code reuse, ease the comprehension of the beam energy transmission inside the BLM electronics, and to avoid one to see this functionality as an obscure black box, which is essential in case of problem tracking.

2 Specifications

2.1 General

This document is in fact describing two (2) different links. In this paper, the term **link** is used for a communication channel between 2 distinct entities. In our case, the first link (L1) is connecting the timing card (designed by *AB–CO*, providing the BEM from measurements) to the BLM combiner card (designed by *Jonathan Emery, AB–BI*). The second link (L2) is broadcasting this energy from the combiner card to the 16 symmetric BLMTC cards (designed by *Christos Zamantzas, AB–BI*) inside the VME crate.

To maximize code reuse and ease maintenance, both links designs are based on the same VHDL code, because both the combiner and the BLMTC cards are hosting the same FPGA. The link specific particularities however, are that L2 is carried on the VME backplane (between P0 connectors), whereas L1 is passing through external cables and daisy-chained to several VME crates.

To understand the particularity of this data path, it is important to keep in mind that the VME crates are specially build for BLM use. Actually, the P2 connectors are not connected to each other on the backplane since no bus lines exists. On the contrary, each of them is connected to a rear side connector, VME64 male standard. Concerning the timing card for example, the BEM data is outputted from the crate through this rear connection with a 50 wire cable. This

choice is made to ensure the 3 other crates to receive the BEM values with the least possible electronics in-between. Furthermore, this gives a first level of fault tolerance, since the BEM values collected on the LHC network are broadcasted to the 3 upward crates via a simple cable.

Here is a simple schematic of the system data path within the lowest VME crate :

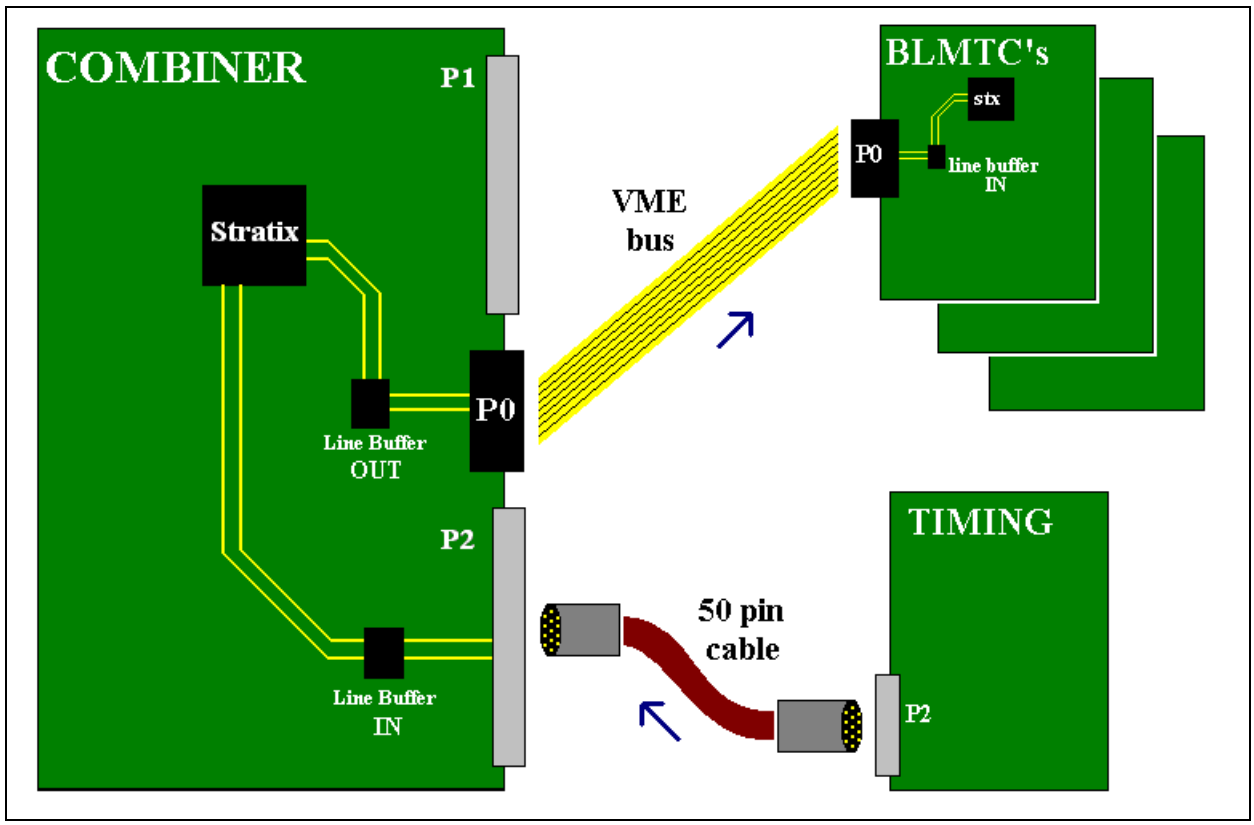

Figure 2.1: *BEM data path inside the first VME crate*

Note that in this drawing the link between the timing card and the combiner (L1) is simplified to a single 50 wire cable. In reality, it is crossing a high voltage rack to be distributed to two other crates. This is to offer the most generic view of the system, enabling us to implement the same code in all the combiner cards.

2.2 Fault Tolerance

2.2.1 Context

As we said in the introduction, energy levels reached in the LHC can be dangerous and damageable for the Collider if the control on the beam is lost. Furthermore, many systems are operating in constrained environments (in terms of fields, radiation or temperature) making them aging prematurely. For these reasons, strict levels of fault tolerance are recommended for essential systems. The BLM electronics are considered as such instruments and should therefore fulfill to these recommendations.

The beam energy value to be processed is a critical issue in the BLM electronics. In the case of a parallel transmission of a value, the fault probability increases with the number of lines used to carry the data on. For this reason, both links are decided to be -quite low data rate-

serial links. Several transmission control features have been included to check the link quality and the data integrity. This will be giving a first level of security during the transmission, but will also be able to give long term statistics on the state of the electronics during the operating period of the LHC.

2.2.2 CRC check

The most famous check function included is the Cyclic Redundancy Check (CRC), which calculates a parity signature on emission and checks at the receiver side if the signature is the same. If this is the case, the frame is considered as valid, else it is simply destroyed. This feature is mainly used to check the instant data integrity, however a big number of successive CRC errors will enable one to suspect hardware failures.

2.2.3 Watchdog timer

Another useful feature to check the link quality is inherent to the serial transmission method. As we will see in the next chapter, the receiver enters in a *RECEIVE* state after reception of a frame start sequence, and gets out of this state after a stop sequence. Asides, to ensure the receiver does not stuck in this state if an error occurs on the line, a watchdog timer is present to tell whether the line is broken. From here we get the information on the line status, broken or active.

2.2.4 Redundancy

To add one more level of fault tolerance to our system, we decided to use the same strategy as the optical links between the tunnel cards and the surface electronics. The links are doubled for a maximum availability in the case of a transmission failure. For semantic reasons and not to confuse with L1 and L2, the redundant wire pair on which the links are carried are called lines (A and B). One link is thus made of two identical lines. In summary, all the transmission control feature listed above are doubled, one for each line.

2.3 Failure levels and tolerances

2.3.1 Transmission (line) Level

At transmission level (lines), the fault tolerence is offered by CRC and time out check. For each received frame, this 2 signals are updated and checked upwards. If one fails (set to ’0’), the frame is dropped. In this case, a signal is propagated to the higher level to inform the system that the considered line is faulty. At this level, no recovery is possible. The only tolerance is offered by giving the information concerning the line transmission control state.

2.3.2 Link Level

The fault tolerance is given at this level of the links, thanks to redundancy. All the transmission equipment is doubled, including transmission lines. If one line is broken or becomes poor in quality, the time out or CRC error flag is recieved, and the active transmission line automatically switches to the redundant one. This is done within 3 ms, corresponding to the watchdog time limit.

The BLM electronics being critical, a backup procedure had to be decided in case of two line breaks. If this happens, no BEM value would be present to process a threshold comparison, leading to a possible unexpected events. The solution is to send the highest beam energy value if this happens, to set the lowest possible thresholds. To ease the comprehention, this behaviour will happen by default when the transmission enters in its *FAULT* state. At link level, the system automatically enters in *FAULT* state when both lines of a link are broken, sending a used definable beam energy value to the next equipement.

2.3.3 BEM level

The previous described features are aimed to secure the data pathes inside the BLM electronics. Of course we have no control on the upward link of the LHC network providing up to date BEM values. But we had to take in account the uneventually possibility that this link also fails. For this, the AB–BT people have included a usefull feature to check if a value is up to date. A specific bit is present in the BEM frame to notify that a received BEM value is up to date. This bit is juste toggling every time a new value is measured and sent. As the BEM update rate is known (around 1 second), another watchdog timer is included to test whether the received value is to be used in the threshold comparators. If this fails, the receiver also enters in its *FAULT* state, sending the default value as described previously.

2.4 Monitoring

For statistical purpose, an error count monitoring function has been added. This enables us to make statistics on the link quality, transmission security, and have a glance on the aging process of the electronics. Two counters are incremented every time an error occurs (timeout and CRC). The values are 16 bits wide, and can be sent to output registers (for remote monitoring), or local LED's on the VME front panel. This is particularly handy for fault tracking and troubleshooting. At the combiner side for example, a global system status could be implemented, taking these link statistics into account.

3 Implementation

3.1 Structure

3.1.1 Frame receiver

The frame transmission is based on Manchester encoding. This type of link is completely synchonous, performing thus robust and safe data transmissions on one single line. The Manchester encoding is also called ”biphase code” because it stores the information in transitions rather then voltage levels. Doing so makes it possible to recover the synchronization clock by decoding a specific frame header with a digital PLL. The links are single direction, and the receivers are doubled for fault tolerance purpose. One particularity is that the redundant lines of the transmission are inverted (symetry).

The manchester decoder block is a reused VHDL entity, written by the AB–CO group. It is slightly modified to fit the BEM transmission specifications. It includes a digital PLL for clock recovery, and is made of a finite state machine. The state is set with the input data. Decoding is launched with a start of frame header, and is stopped after reception of a complete frame.

Just after the decoder is wired the CRC calculator and comparator. As said before, two status flags are present to notify errors in the CRC or the watchdog, and the toggle bit is also outputted to check the update status of the BEM values.

3.1.2 Frame transmitter

The frame transmitter is also borowed from AB–CO, and is paired with the receiver. Its frame rate is 1 frame per ms (after revision of 28 November 2006 by *Nicolas Voumard, AB–BT*. The bitrate clock inside the frame is 1 MHz. The frame is 32 bits long and structured as following:

1. ”10010000” header (8 bits)
2. Energy value (16 bits)
3. Toggle bit + ”000” (4 bits)
4. CRC (4 bits)

The CRC calculator generates a signature on the 28 data bits at once, and the generating polynom is $1 + x + x^4$. These 4 bits are added to the 28 data bits to complete a 32 bit frame. After this step, the whole frame is given to a Manchester encoder, which sends the data through de link. Two of these transmitters are sending data on different lines. One of this line however is inverted before sending, to give a minimum crosstalk immunity on twisted pairs.

3.1.3 BEM receiver module

The BEM receiver module is the entity composed of the 2 redundand line receivers, le line switch (*line_selector*) and a watchdog timer monitoring the toggle bit. These components have

been brought together in one block to ease the taem work between the designers of the BLM electronics, as the links are envolved in various parts. Each members work is then to place the files in the hierarchy tree, and bind the different I/O's together. Here is a RTL view of the receiver module:

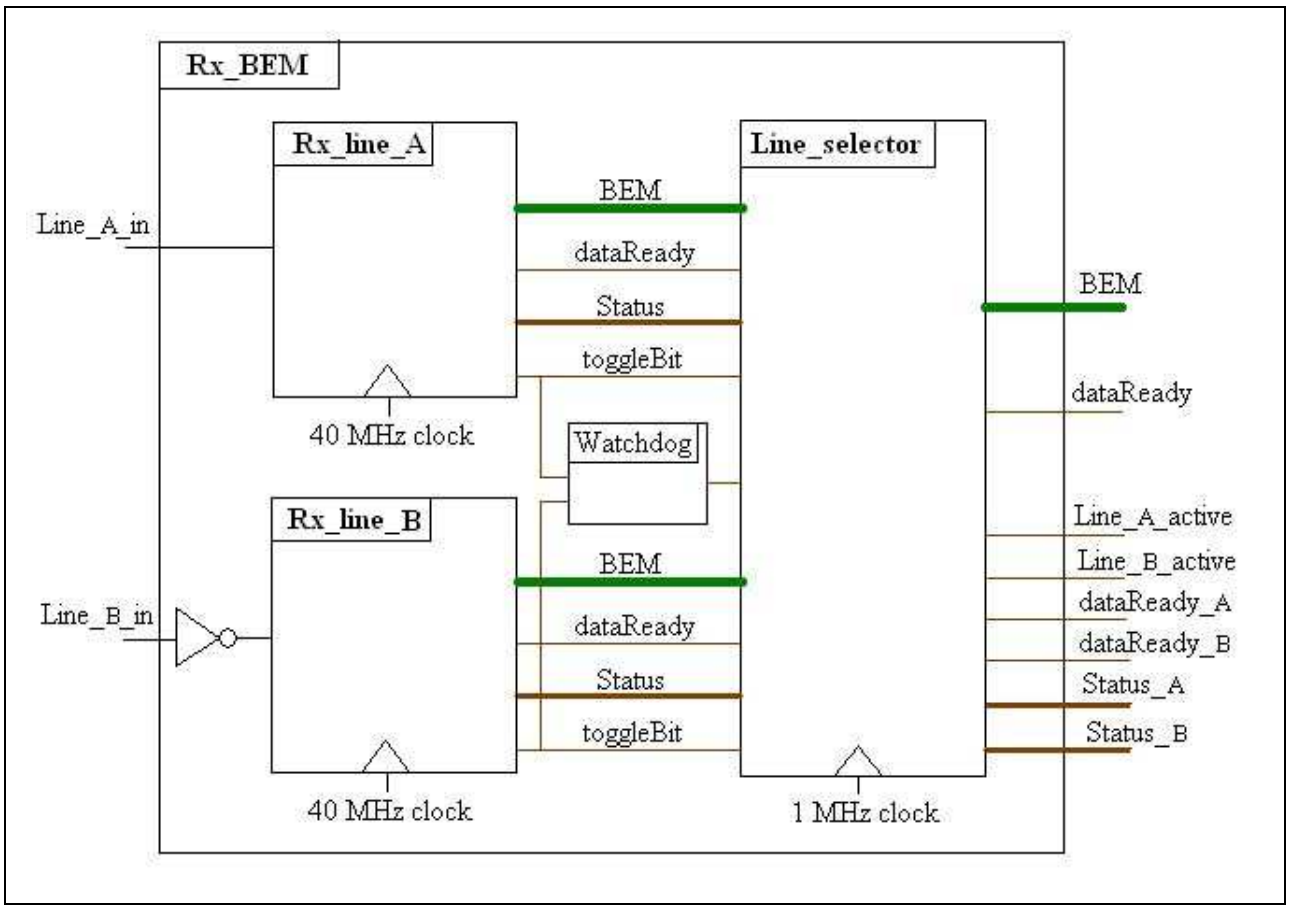

Figure 3.1: *RTL view of the BEM receiver module*

Concerning the I/O's, this module needs 2 clock inputs. This is for space optimisation purpose, because both are already available in the host design. This avoids generating another 1 MHz clock with a counter. Furthermore, the BEM value is outputted in 16 bit format, and the other outputs are for statistics purpose. These makes it possible to count the number of frames, the CRC and the time out errors, and to show which line is actually active.

3.2 Files and hierarchy

3.2.1 Transmitter

This side of the links is made out of 2 entities. The first is the Manchester encoder (refered to with component *me2*). The second is bringing together this component with a CRC generation function, in the same architecture. The needed files to be able to synthesize the transmitter are :

- me2.vhd
- EnergyBroadcast.vhd
- BEM_pck.vhd

This last file contains the global constants needed to configure the entity, like bitrate, framerate, initial configuration registers values and bus widths.

3.2.2 Receiver

The receivers hierarchy is a bit more complex the transmitter, because of the many added function relative to fault tolerance. The main squeletton is the one seen in figure 3.1. However, many sub-stages are present in the hierarchy.

- BEM_serial_receiver.vhd (Line receivers)
  - BEM_watchdog.vhd (3 ms watchdog)
  - BEM_crc (CRC generator)
  - mdMilRegSynchRst.vhd (Manchester decoder)
  - mddef.vhd (configuration registers for the Manchester decoder)
- link_selector.vhd (line switching FSM for redundancy)
- selector_watchdog.vhd (watchdog monitoring the toggle bit)
- BEI_pck.vhd (global constants package)

3.3 Global constants

As usual in multiple entities designs, a package is containing global constants, which are propagating to every individual blocks during synthesis. In the receiver block, this package is called *BEI_pck*, and is located in the file with the same name. This is a list of constants needed to be set to obtain a correct synthesis.

```
-- reset level
   CONSTANT RESET_ACTIVE : std_logic := '1';

-- BEM watchdog time out, here 3 ms
   CONSTANT BEMWD_TIMELIM : std_logic_vector(19 downto 0) := X"1D4C0";

-- Default value to send if a problem in the link occurs
   CONSTANT MAX_BEM : std_logic_vector := "1010101001010101";

-- Framerate in microseconds
   CONSTANT FRAME_RATE_TIME : natural := 500;

-- after this time the upward (before timing module) link is considered broken (toggling test)
   CONSTANT MAX_TOGGLE_TIME : natural range 0 to 3000000 := 2500000;
```

The important constants to specify are the *MAX_BEM* and the *MAX_TOGGLE_TIME*. The first one is the default value sent to the BLM electronics in case of link break. According to the defined emergency procedure, this corresponds to the maximum energy value, corresponding to the minimum thresholds to apply.

The second important value is the time after which the upward link (distributing BEM values) is considered broken. After this time out (given in microseconds) the default value is sent to the BLM electronics.

3.4 Fault tolerance scheme

The fault tolerance is based on redundancy. Two lines for each link are providing the BEM data, but only one is effectively used for the transmission. The other one is a ”hot spare” being used if the first line fails. This switch is done automatically on fail of the active link, within 3 miliseconds. The fails include CRC error (line transmission error) and receiver time out (line broken). This is achieved with a generic finite state machine. Here is its state transission scheme:

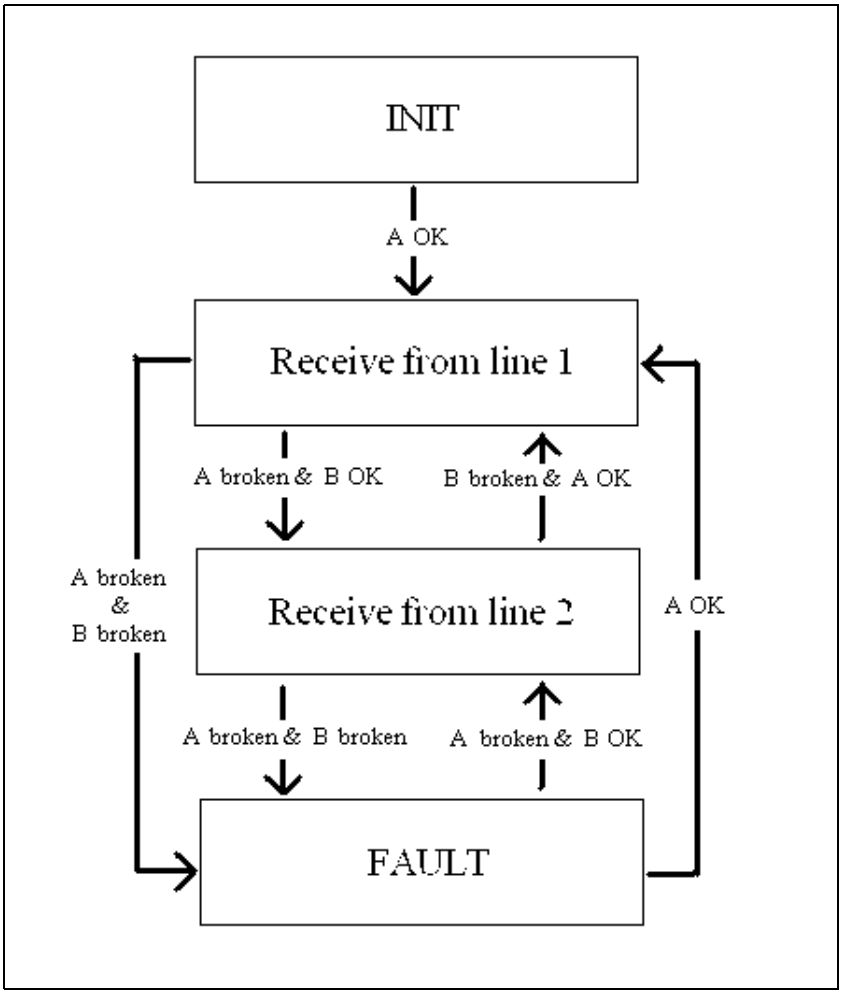

Figure 3.2: *State diagram of fault tolerance FSM*

As we can see on this scheme, the initial state is left only if line A is OK. This is to give a defined start point to the FSM. In the same way, the line A is prefered when the FSM exits the *FAULT* state, and when both lines are OK again at the same moment.

A *FAULT* state is also triggered regardless from this scheme when no (update) bit toggling occured for more than the specifeid value in the global constants package. This value should be set around one second, as this is the planned update rate of the BEM values. (See AB–CO timing distribution specifications)