# MEMORY MAPPING BLECS

| OVERVIEW | 0 | 7FFFFF |
|---|---|---|

| Description | Start | End | Comments |
|---|---|---|---|
| PM SRAM | 0 | 200000 | |
| BD SRAM | 200000 | 400000 | |
| Xtra SRAM | 400000 | 600000 | |
| Flash ROM | 600000 | 700000 | |
| LOGIN | 700000 | 701FFF | |
| SPARE | 702000 | 71FFFF | |
| TEST RESULTS | 720000 | 721FFF | |
| SPARE | 722000 | 7DFFFF | |
| Control Registers | 7E0000 | 7EFFFF | |
| DAB64x Control / Status Registers | 7F0000 | 7FFFFF | |

# MEMORY MAPPING BLECS

| LOGIN | 700000 | 70FFFF |
|---|---|---|

| Description | Start | End | Bit | Comments | Alarms | MUX FPGA |
|---|---|---|---|---|---|---|
| System level | 700000 | | 31 | System operational (SYS.OP) | | 4 |
| | | | 30 | System under test (TEST) | | |
| | | | 29 | Test requested (T.REQ) | | |
| | | | 28 | Post Mortem (PM) | | |
| | | | 27 | High voltage fault (HV) | | |
| | | | 26 | Beam Energy fault (BE) | | |
| | | | 25 | Orbit Clock fault (ORBCK) | | |
| | | | 24 | Dump occured (DUMP) | | |
| | | | 23 | User System test pending | | |
| | | | 22 | User Consistency test pending | | |
| | | | 21 | User Threshold to BPL pending | | |
| | | | 20 | User Energy Test pending | | |
| | | | 19 | User BPBIS (BLECS to Beam interlock) pending | | |
| | | | 18 | Expert System test pending | | |
| | | | 17 | Expert Consistency test pending | | |
| | | | 16 | Expert Threshold to BPL pending | | |
| | | | 15 | Expert Energy Test pending | | |
| | | | 14 | Expert BPBIS (BLECS to Beam interlock) pending | | |
| | | | 13 | Expert BPTC (Beam Permit BLETC to BLECS) pending | | |
| | | | 12 | Expert HVLF test pending | | |
| | | | 11 | Expert HVCFC (100 pA test) pending | | |
| | | | 10 | Expert HVRDAC (Dac Reset) pending | | |
| | | | 9 | Expert HVGOH (GOH Reset) pending | | |
| | | | 8 | Expert Manual control Request pending | | |
| | | | 7 | Timer System Test pending | | |
| | | | 6 | Timer System test request normal | | |
| | | | 5 | Timer System test request Priority (BP away next Dump) | | |
| | | | 4..0 | SPARE | | |
| Next system test request | 700004 | | | time in second remained before normal system test | | 5 |
| Next critical system test request | 700008 | | | time in second remained before cricical system test | | 6 |
| Active tests overview | 70000C | | 31 | SYSTEM TEST | | 7 |
| | | | 30 | CONSISTENCY (threshold table control) | | |
| | | | 29 | THRESHOLD to BPL | | |
| | | | 28 | ENERGY TEST | | |
| | | | 27 | BPBIS(Beam Permit to the LBIS) BLECS -> LBIS | | |
| | | | 26 | BPTC(Beam Permit BLETC to BLECS) BLETC -> BLECS | | |
| | | | 25 | HVLF (Modulation) | | |
| | | | 24 | HVTCFC (Test CFC) | | |
| | | | 23 | HVRDAC (DAC RESET) | | |
| | | | 22 | HVRGOH (GOH REST) | | |
| | | | 21 | MANUAL CONTROL | | |
| | | | 20..0 | SPARE | | |
| Result of last test system 1 | 700010 | | | Time in seconde since the last test | | 8 |
| Result of last test system 2 | 700014 | | 31 | SYSTEM TEST was successful | | 9 |
| | | | 30 | CONSISTENCY was successful | | |
| | | | 29 | THRESHOLD to BPL was successful | | |
| | | | 28 | SPARE | | |
| | | | 27 | SPARE | | |
| | | | 26 | BPTC was successful | | |
| | | | 25 | HVLF was successful | | |
| | | | 24 | HVTCFC(Test CFC) | | |
| | | | 23..0 | SPARE | | |
| Time | 700018 | | | Time in seconde since the last reset of the board | | 10 |
| User Beam Permit | 70001C | | 31 | TC Unmaskable | | 11 |
| | | | 30 | TC Maskable | | |
| | | | 29 | IN Unmaskable A from upper Combiner | | |
| | | | 28 | IN Unmaskable B | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | 27 | IN Maskable A | | |
| | | | 26 | IN Maskable B | | |
| | | | 25 | OUT Unmaskable A To lower Combiner | | |
| | | | 24 | OUT Unmaskable B | | |
| | | | 23 | OUT Maskable A | | |
| | | | 22 | OUT Maskable B | | |
| | | | 21 | Beam info A | | |
| | | | 20 | Beam info B | | |
| | | | 19 | Beam info A had respond to last BLECS-DUMP | | |
| | | | 18 | Beam info B had respond to last BLECS-DUMP | | |
| | | | 17 | SPARE | | |
| | | | 16 | SPARE | | |
| | | | 15..8 | Unmascable Dump counter since last reset | | |
| | | | 7..0 | Mascable Dump counter since last reset | | |
| Turn counter when last dump | 700020 | | | 32 bits counter | | 12 |
| Bunch counter when last dump | 700024 | | 11..0 | 12 bits counter | | 13 |
| Beam Energy | 700028 | | 31..16 | Beam Energy In | | 14 |
| | | | 15..11 | Beam Energy Out | | |
| | | | 10 | Beam Energy error | | |
| | | | 9..5 | Beam Energy spare bits | | |
| | | | 4 | Beam permit line test activation | | |
| | | | 3..0 | Beam permit line test TC card number | | |
| | 70002C | | | Frame counter channel A | | 15 |
| | 700030 | | | Frame counter channel B | | 16 |
| | 700034 | | | CRC error reception channel A from the CTRV | Threshold | 17 |
| | 700038 | | | CRC error reception channel B from the CTRV | Low level if Error>5/s | 18 |
| | 70003C | | | Time out channel A from the CTRV | Threshold | 19 |
| | 700040 | | | Time out channel B from the CTRV | Medium level if Error>5/s | 20 |
| | 700044 | | | Time Out Beam Energy Value | | 21 |
| High Voltage 1 survey | 700048 | | 31 | HV1 voltage higher | if high | 22 |
| | | | 30 | HV1 voltage lower | if high | |
| | | | 29 | HV1 current higher | if high | |
| | | | 28 | HV1 current lower | if high | |
| | | | 27..24 | SPARE | | |
| | | | 23..0 | HV1 voltage value (24 bits) [HV = 10/2**24*code*300] in V | | |
| High Voltage 2 survey | 70004C | | 31 | HV2 voltage higher | if high | 23 |
| | | | 30 | HV2 voltage lower | if high | |
| | | | 29 | HV2 current higher | if high | |
| | | | 28 | HV2 current lower | if high | |
| | | | 27..24 | SPARE | | |
| | | | 23..0 | HV2 voltage value (24 bits) [HV = 10/2**24*code*300] in V | | |
| High Voltage Currents | 700050 | | 31..16 | HV1 current value (16 bits) [I = code/2**16*20] in mA | | 24 |
| | | | 15..0 | HV2 current value (16 bits) [I = code/2**16*20] in mA | | |
| VME Voltages | 700054 | | 31..29 | SPARE | | 25 |
| | | | 28..16 | VME 3V3 (13 bits) with 10V full scale | | |
| | | | 15..13 | SPARE | | |
| | | | 12..0 | VME 5V (13 bits) with 10V full scale | | |
| Analog Voltages | 700058 | | 31..29 | SPARE | | 26 |
| | | | 28..16 | Analog 5V (13 bits) with 10V full scale | | |
| | | | 15..13 | SPARE | | |
| | | | 12..0 | Analog 5V reference (13 bits) with 10V full scale | | |
| Low Voltage survey | 70005C | | 31 | LV Analog 5V ok | | 27 |
| | | | 30..0 | LV Analog 5V ripples counter | | |
| | 700060 | | 31 | LV Analog ±15V ok | | 28 |
| | | | 30..0 | LV Analog ±15V ripples counter | | |
| | 700064 | | 31 | LV Digital 3.3V ok | | 29 |
| | | | 30..0 | LV Digital 3.3V ripples counter | | |
| | 700068 | | 31 | LV Digital 5V ok | | 30 |
| | | | 30..0 | LV Digital 5V ripples counter | | |
| | 70006C | | 31 | LV Digital ±12V ok | | 31 |
| | | | 30..0 | LV Digital ±12V ripples counter | | |

# MEMORY MAPPING BLECS

| TEST RESULTS | 720000 | 72FFFF |
|---|---|---|

| Description | Start | End | Bit | Comments |
|---|---|---|---|---|
| High Voltage test SETUP | 720000 | 720003 | 31..16 | HVTCFC (Test CFC) HV applied in case of this test |
| | | | 15..0 | HVRDAC (RESET DAC) HV applied in case of this action |
| | 720004 | 720007 | 31..16 | HVRGOH (RESET GOH) HV applied in case of this action |
| | | | 15..0 | SPARE |
| BPLTC (Beam Permit Lines) from TC | 720008 | 72000B | 32 | TC Board 1 present (1=yes, 0=no) |
| | | | 31 | TC Board 2 present |
| | | | … | … |
| | | | 16 | TC Board 16 present |
| | | | 15 | BPLTC result TC 1 (1=passed, 0=not passed) |
| | | | 14 | BPLTC result TC 2 |
| | | | … | … |
| | | | 0 | BPLTC result TC 16 |
| **HVLF SETUP** | | | | |
| Modulation | 72000C | 72000F | 31..16 | Mod amplitude at the output of the DAC |
| | | | 15..0 | Frequency Divider [f = 1MHz/256/fd] |
| | | | | |
| Modulation | 720010 | 720013 | 31..24 | digital multiplicator (FPGA internal factor) |
| | | | 23..16 | attenuation digital pot 1 |
| | | | 15..8 | attenuation digital pot 2 |
| | | | 8..0 | SPARE |
| Offset voltage | 720014 | 720017 | 31..16 | offset voltage at the output of the DAC |
| | | | 15..0 | SPARE |
| | | | | |
| Decision criteria immediate test | 720018 | 72001B | 32..16 | Amplitude min to say channel x is connected |
| | | | 15..0 | SPARE |
| **HVLF RESULTS** | | | | |
| Time | 72001C | 72001F | | Time MSDW |
| | 720020 | 720023 | | Time LSDW |
| overview | 720024 | 720027 | 31 | AutoTest done (1=yes, 0=never since last reset) |
| | | | 30 | AutoTest result |
| | | | 29..25 | Number of tested TC |
| | | | 24..16 | Number of tested channels |
| | | | 15..0 | TC test passed (MSBit TC1) 1=passed 0=failed |
| Channel 1 | 720028 | 72002B | 31 | Test passed |
| | | | 30..16 | amplitude immediate test (15 bits) |
| | | | 15..0 | phase immediate test (16 bits) |
| | 72002C | 72002F | 31..16 | long term test sin factor Ryx_s |
| | | | 15..0 | long term test cos factor Ryx_c |
| Channel 2 | 720030 | 720033 | | 2x 32bits data |
| … | … | … | … | … |
| Channel 256 | 720820 | 720823 | | 2x 32bits data |
| | | | | |

# MEMORY MAPPING BLECS

| Control Registers | 7E0000 | 7EFFFF |
|---|---|---|

| Description | Start | End | Bit | Comments | MUX FPGA | Utility |
|---|---|---|---|---|---|---|
| | | | | | | |
| Tests Request | 7E0000 | | 31 | User System test | 40 | |
| | | | 30 | User Consistency test | | |
| | | | 29 | User Threshold to BPL test | | |
| | | | 28 | User Energy Test | | |
| | | | 27 | User BPBIS (BLECS to Beam interlock) | | |
| | | | 26 | Expert System test | | |
| | | | 25 | Expert Consistency test | | |
| | | | 24 | Expert Threshold to BPL test | | |
| | | | 23 | Expert Energy Test | | |
| | | | 22 | Expert BPBIS (BLECS to Beam interlock) | | |
| | | | 21 | Expert BPTC | | |
| | | | 20 | Expert HVLF test | | |
| | | | 19 | Expert HVCFC (100 pA test) | | |
| | | | 18 | Expert HVRDAC (Dac Reset) | | |
| | | | 17 | Expert HVGOH (GOH Reset) | | |
| | | | 16 | Expert Manual control Request | | |
| | | | 16..0 | SPARE | | |
| Manual Control | 7E0004 | | 31 | Expert Manual control activation (only after "System under test" and "Manual control" status are high) | | |
| | | | 30 | Send command to TC: Force dump event on specific TC | | Used for the test : BPLTC (BLETC to BLECS) |
| | | | 29..26 | TC Number for forced dump | | |
| | | | 25 | Choose Energy to send to TC | | Used for the test : Consistency |
| | | | 24..20 | Energy value to be send | | |
| | | | 19 | Force Dump event Unmascable | | |
| | | | 18 | Force Dump event Mascable | | |
| | | | 17 | Force Beam Permit (Mascable & Unmascable) Lines individually | | BPBIS (BLECS to CIBU) Only visual check on the CIBU leds Should be done in the 4 BLECS at the same time to see result if xA 'true' xB is forced 'false' autom. |
| | | | 16 | Force Beam Permit UA | | |
| | | | 15 | Force Beam Permit UB | | |
| | | | 14 | Force Beam Permit MA | | |
| | | | 13 | Force Beam Permit MB | | |
| | | | 12..0 | SPARE | | |
| Present TC board table | 7E0008 | | 31..16 | (MSBit = BLETC nbr. 1) '1'=present, '0'=no board | 42 | Beam permit BLETC to BLECS |
| | | | 16..0 | SPARE | | |
| Status HV of the BLECF | 7E000C | | | TC 1 & TC 2 Status HV (MSBit = channel 1) | 43 | |
| Status TESTCFC of the BLECF | 7E0010 | | | TC 1 & TC 2 Status TESTCFC (MSBit = channel 1) | 44 | |
| Status RSTDAC of the BLECF | 7E0014 | | | TC 1 & TC 2 Status RSTDAC (MSBit = channel 1) | 45 | |
| Status RSTGOH of the BLECF | 7E0018 | | | TC 1 & TC 2 Status RSTGOH (MSBit = channel 1) | 46 | |
| SPARE | 7E001C | 7E00FF | | | | |
| Present channels table | 7E0100 | | | TC 1 & TC 2 Present Channels (MSBit = channel 1) | 47 | |
| | 7E0104 | | | TC 3 & TC 4 '1' = The channel is connected to a IC | | |
| | 7E0108 | | | TC 5 & TC 6 | | |
| | 7E010C | | | TC 7 & TC 8 | | Modulation test |
| | 7E0110 | | | TC 9 & TC 10 | | |
| | 7E0114 | | | TC 11 & TC 12 | | Update at the startup and at every change |
| | 7E0118 | | | TC 13 & TC 14 | | |
| | 7E011C | | | TC 15 & TC 16 | | |
| SPARE | 7E0120 | 7E0FFF | | | | |
| Running Maximum N°7 table | 7E1000 | | | Channel 1 (TC 1) Running Maximum N°7 | 48 | |
| | 7E1004 | | | Channel 2 (TC 1) | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | … | | Modulation test<br><br>Update every login (1s) when HVLF test is active<br><br>when "System under test" = '1' |
| | | | | Channel 16 (TC 1) | | |
| | | | | CH17-CH32 (TC 2) | | |
| | | | | CH33-CH48 (TC 3) | | |
| | | | | … | | |
| | | | | Channel 240 (TC 16) | | |
| | | | | Channel 241(TC 16) | | |
| | | | | … | | |
| | 7E13FC | | | Channel 256 (TC 16) | | |
| Default HVLF Control 1 | 7E1400 | | 31..16 | Bias Voltage in dac values [V = 10/2**16*dacValue*300] | 49 | |
| | | | 15..8 | Modulation analog attenuator [Total = 100+Att/256*400] | | |
| | | | 7..0 | Modulation digital multiplicator [V = 11.72*DigitalMultiplicator] | | |
| Default HVLF Control 2 | 7E1404 | | 31..16 | SPARE | 50 | |
| | | | 15..0 | Modulation frequency division [F = 10e6/2048/FrequDivision] | | |
| Default HV values 1 | 7E1408 | | 31..16 | Bias Voltage Normal Operation | 51 | In DAC values<br>[Vhv = 10/2**16*dacValue*300] |
| | | | 15..0 | Bias Voltage HVCFC (100 pA test) | | |
| Default HV values 2 | 7E140C | | 31..16 | Bias Voltage HVRDAC (Dac Reset) | 52 | |
| | | | 15..0 | Bias Voltage HVGOH (GOH Reset) | | |

# MEMORY MAPPING BLECS

| DAB64x Control Status Registers | 7F0000 | 7FFFFF |
|---|---|---|

| Description | Start | End | data (x32bits) | Comments |
|---|---|---|---|---|
| Flash ROM Control/Status | 7F0000 | 7F0004 | 1 | |
| Revision ADC 0 | 7F0004 | 7F0005 | 0.25 | byte0 - 0x7F0004 - Revision ADC High byte |
| Revision ADC 1 | 7F0005 | 7F0006 | 0.25 | byte1 - 0x7F0005 - Revision ADC Low byte |
| Revision ADC 3 4 | 7F0006 | 7F0008 | 0.5 | reserved |
| SPARE | 7F0008 | 7F0014 | 3 | |
| Revision Letter/Date 0 | 7F0014 | 7F0015 | 0.25 | byte0 - 0x7F0014 - Revision Letter |
| Revision Letter/Date 1 | 7F0015 | 7F0016 | 0.25 | byte1 - 0x7F0015 - Revision Date MM |
| Revision Letter/Date 2 | 7F0016 | 7F0017 | 0.25 | byte2 - 0x7F0016 - Revision Date DD |
| Revision Letter/Date 3 | 7F0017 | 7F0018 | 0.25 | byte3 - 0x7F0017 - Revision Date yy |
| Monitor Temp/Power 0 | 7F0018 | 7F0019 | 0.25 | byte0 - 0x7F0018 - STRATIX Temp High byte |
| Monitor Temp/Power 1 | 7F0019 | 7F001A | 0.25 | byte1 - 0x7F0019 - STRATIX Temp Low byte |
| Monitor Temp/Power 2 | 7F001A | 7F001B | 0.25 | byte2 - 0x7F001A - HWBTN Power Monitor Status |
| Monitor Temp/Power 3 | 7F001B | 7F001C | 0.25 | byte3 - 0x7F001B - VWBTN Power Monitor Status |
| SPARE | 7F001C | 7F003C | 8 | |
| Serial Number MSB 0 | 7F003C | 7F003D | 0.25 | byte0 - 0x7F003C - Serial Number Upper 4 bytes |
| Serial Number MSB 1 | 7F003D | 7F003E | 0.25 | byte1 - 0x7F003D |
| Serial Number MSB 2 | 7F003E | 7F003F | 0.25 | byte2 - 0x7F003E |
| Serial Number MSB 4 | 7F003F | 7F0040 | 0.25 | byte3 - 0x7F003F |
| Serial Number LSB 0 | 7F0040 | 7F0041 | 0.25 | byte0 - 0x7F0040 - Serial Number Lower 4 bytes |
| Serial Number LSB 1 | 7F0041 | 7F0042 | 0.25 | byte1 - 0x7F0041 |
| Serial Number LSB 2 | 7F0042 | 7F0043 | 0.25 | byte2 - 0x7F0042 |
| Serial Number LSB 3 | 7F0043 | 7F0044 | 0.25 | byte3 - 0x7F0043 |
| SPARE | 7F0044 | 7F0050 | 3 | |
| PM SRAM Read Pointer | 7F0050 | 7F0054 | 1 | MSB 1/0 for full/partial read |
| BD SRAM Read Pointer | 7F0054 | 7F0058 | 1 | MSB 1/0 for full/partial read |
| Xtra SRAM Read Pointer | 7F0058 | 7F005C | 1 | MSB 1/0 for full/partial read |
| SPARE | 7F005C | 7F0100 | 41 | |
| Collimation Data - Ch 01 | 7F0100 | 7F0104 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 02 | 7F0104 | 7F0108 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 03 | 7F0108 | 7F010C | 1 | 32 values deep FIFO |
| Collimation Data - Ch 04 | 7F010C | 7F0110 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 05 | 7F0110 | 7F0114 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 06 | 7F0114 | 7F0118 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 07 | 7F0118 | 7F011C | 1 | 32 values deep FIFO |
| Collimation Data - Ch 08 | 7F011C | 7F0120 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 09 | 7F0120 | 7F0124 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 10 | 7F0124 | 7F0128 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 11 | 7F0128 | 7F012C | 1 | 32 values deep FIFO |
| Collimation Data - Ch 12 | 7F012C | 7F0130 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 13 | 7F0130 | 7F0134 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 14 | 7F0134 | 7F0138 | 1 | 32 values deep FIFO |
| Collimation Data - Ch 15 | 7F0138 | 7F013C | 1 | 32 values deep FIFO |
| Collimation Data - Ch 16 | 7F013C | 7F0140 | 1 | 32 values deep FIFO |
| Collimator Data Overflow | 7F0140 | 7F0144 | 1 | Register |
| SPARE | 7F0144 | 7FC000 | 12207 | |
| BLM Logging Memory A | 7FC000 | 7FC200 | 128 | used for the First 8 detectors |
| BLM Logging Memory B | 7FC200 | 7FC400 | 128 | used for the Second 8 detectors |
| BLM ESL Memory A | 7FC400 | 7FC440 | 16 | used for the First 8 detectors |
| BLM ESL Memory B | 7FC440 | 7FC480 | 16 | used for the Second 8 detectors |
| BLM ESL Memory (ADC RANGE) | 7FC480 | 7FC500 | 32 | Calculated ADC RANGE for all detectors |
| BLM Th Memory A | 7FC500 | 7FC700 | 128 | used for the First 8 detectors |
| BLM Th Memory B | 7FC700 | 7FC900 | 128 | used for the Second 8 detectors |
| SPARE | 7FC900 | 800000 | 3520 | |