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the
Large
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project

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[SPEC]

BLECS "COMBINER" TECHNICAL SPECIFICATION

Abstract

In the context of the LHC, the Beam Loss Monitoring Section needs to design a VME card called BLECS (Combiner and Survey) also called "Combiner" to work with the BLETC (Thresholds Comparators) card and the rest of the system. It purpose is to propagate the Beam Energy and the Beam Permits signals, control and survey the high voltage supply of the ionization chambers as well as the low voltage on the VME create. These signals passes through the P0 and P2 connectors on the VME backplane independantly of the CPU for critical resons.

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History of Changes

Rev. No.	*Date*	*Pages*	*Description of Changes*

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1. INTRODUCTION

In the context of the LHC, the Beam Loss Monitoring Section needs to design a VME card called BLECS (Combiner and Survey) also called "Combiner" to work with the BLETC (Thresholds Comparators) card and the rest of the system. It purpose is to propagate the Beam Energy and the Beam Permits signals, control and survey the high voltage supply of the ionization chambers as well as the low voltage on the VME create. These signals passes through the P0 and P2 connectors on the VME backplane independantly of the CPU for critical resons.

2. WHERE THE COMBINER TAKE PLACE

There will be one combiner per VME create for a total of 25 cards. The combiner connect the different VME create located on the same armoire in daisy chain technics as shown on the figure 1 (old version).

The combiner should:

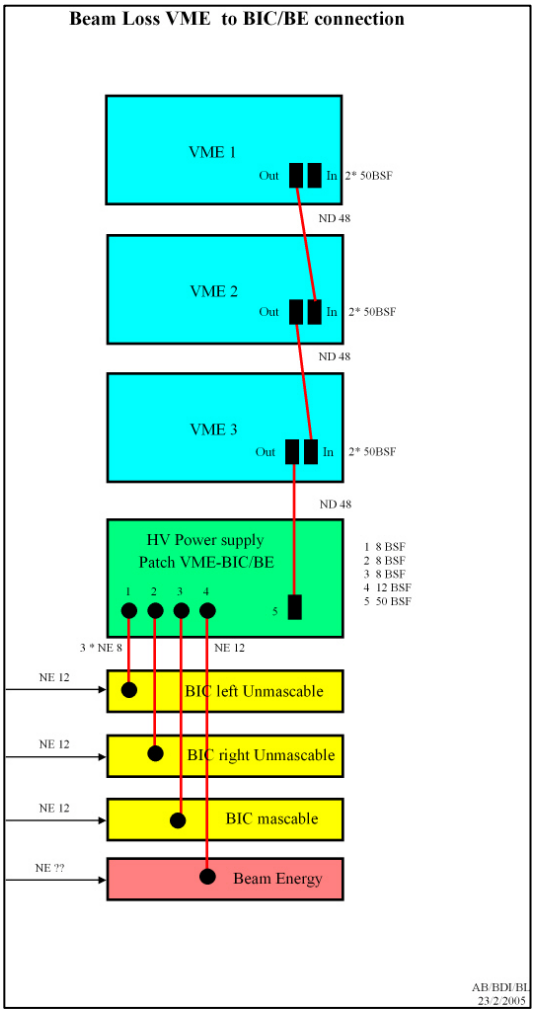
1) Send the beam energy to the TC cards in order to have the correct thresholds table.

2) Receive and transmit the beam permit from the TC card to the BIS and time stamp the event with the turn mumber given by the BOBBR.

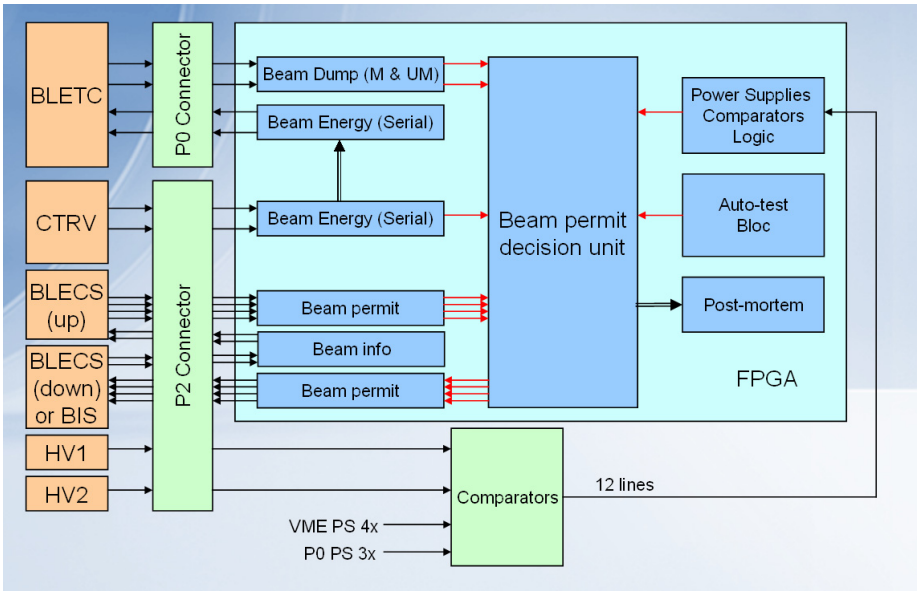
3) Monitor the power supplies of the VME backbone and report fault and ripples.

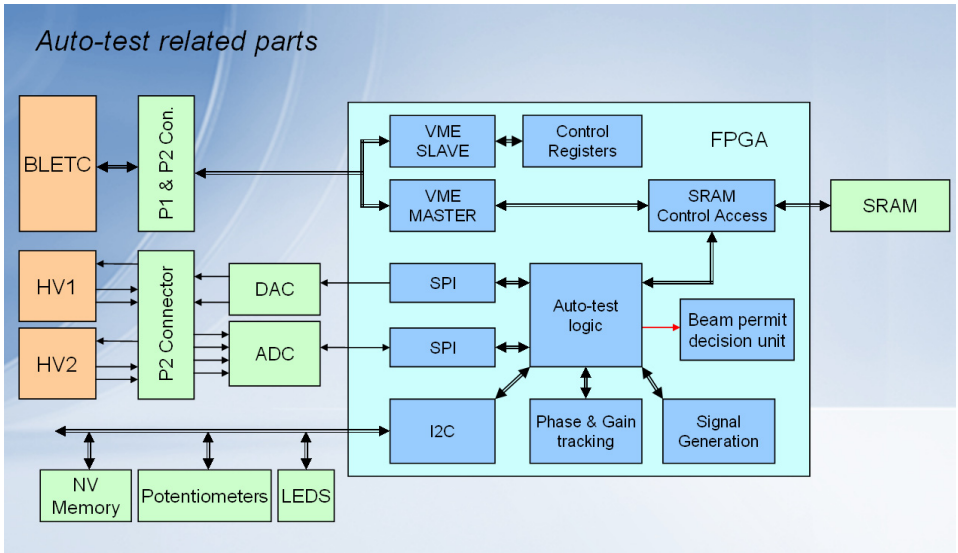
4) Control and survey the high voltage going to the ionisation chambers and report fault.

5) Initiate and realize the test of the cabling to check the entire acquisition chain from the high voltage supply to the TC.



3. FUNCTIONNALITIES OF THE COMBINER

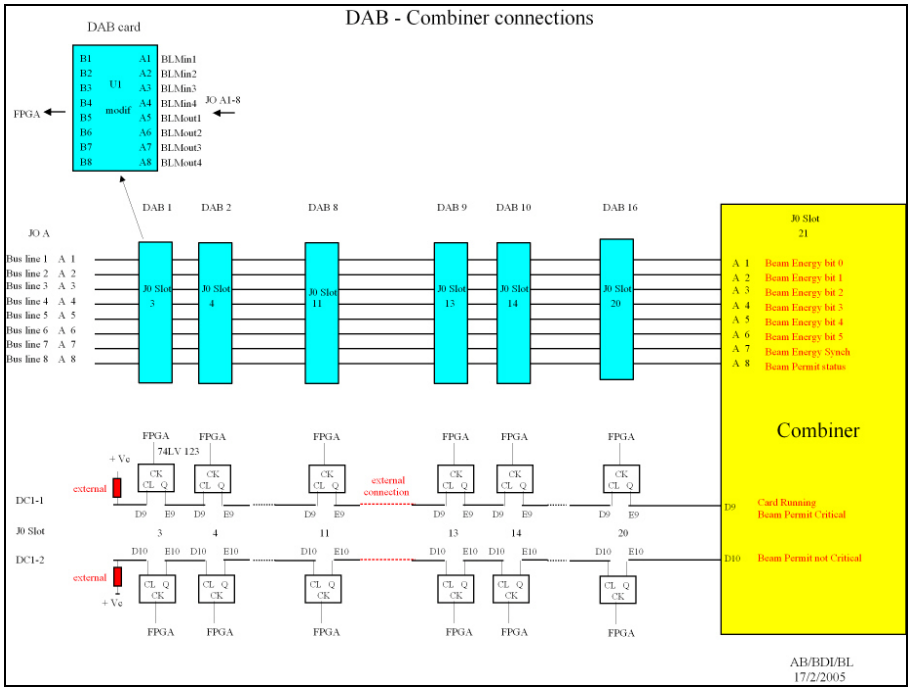




3.1 PROPAGATE THE BEAM ENERGY TO THE TC & COLLECT THE BEAM PERMIT

The TC card needs the energy level in order to load the correct thresholds tables. The information is received from AB-CO with the CTRV through the P0 connector with 2 redundant serial lines. The packet are received every millisecond, the energy level is updated every second on the AB-CO network.

Another important function is to transmit the beam permit lines from the TC to the BIC system. If a TC detect a higher level than it threshold, one of the 2 lines "Beam permit" goes to low and the combiner has to transmit it to the BIC system. There are 2 different level of beam permit (Beam permit critical and Beam permit not critical)



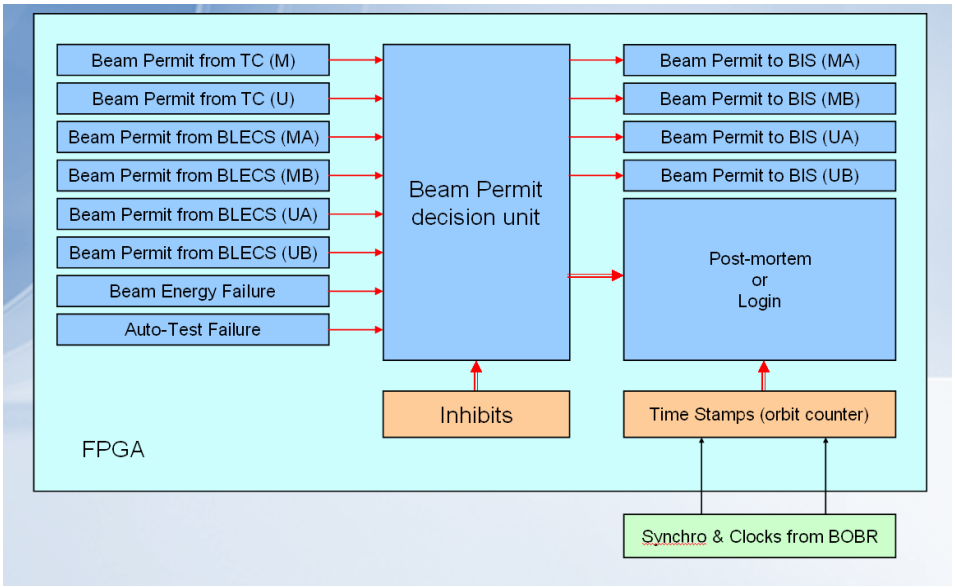
3.2 TRANSMIT THE BEAM PERMIT TO THE BIS

Inputs BP_X_X are the complementary, '0' means the beam is permitted

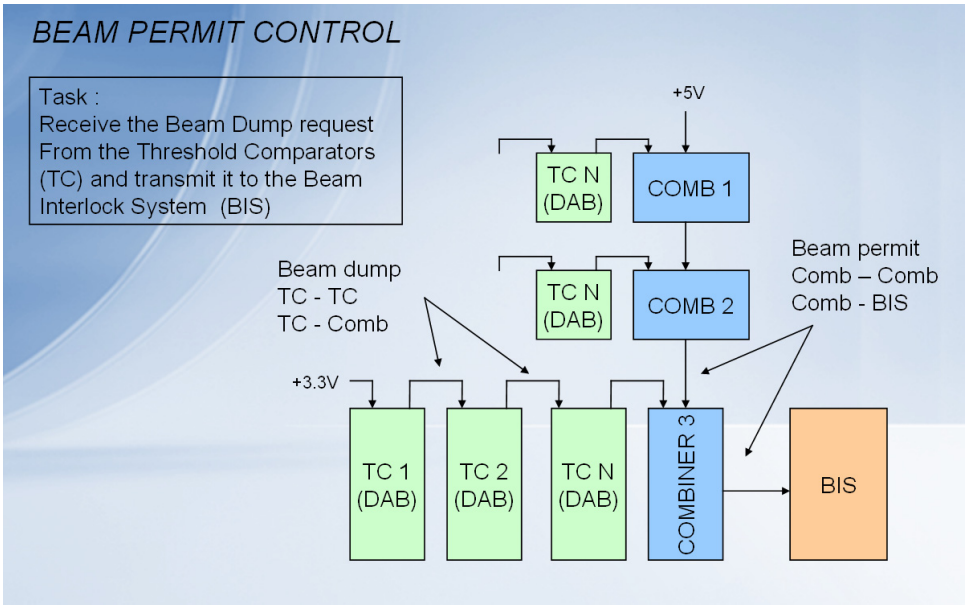
Outputs BP_X_X are going directly to the one shoot. A frequency >1MHz will retrigger it constantly => output = 1 and the beam is permitted. If BP_X_X is 1 or 0 constant, the output = 0 and the beam permit is away.

INPUTS						OUTPUTS			
M_TC	U_TC	BP_M_A	BP_M_B	BP_U_A	BP_U_B	BP_M_A	BP_M_B	BP_U_A	BP_U_B
1	1	0	0	0	0	5MHz	5MHz	5MHz	5MHz
x	x	x	x	x	1	5MHz	5MHz	0	0
x	x	x	x	1	x	5MHz	5MHz	0	0
x	0	x	x	x	x	5MHz	5MHz	0	0
x	x	x	1	x	x	0	0	5MHz	5MHz
x	x	1	x	x	x	0	0	5MHz	5MHz
0	x	x	x	x	x	0	0	5MHz	5MHz

When the beam permit from the TC goes to low, the combiner has to propagate this information to the BIS in order to initiate a beam dump if needed. The event is also time stamped with the turn number for post mortem purpose.



There is only one user beam permit interface for 3 create. The combiner of the top create transmit to the one below. The second combiner (middle one) transmits to the last one. Then the last one transmits it to the beam permit interface. The combiners don't know where they send the beam permits because the links from combiner to combiner and combiner to BIS are the same nature.



Theses signals below transit thought all combiner of the armoire (3 crates) in a daisy chain scheme and then are transmitted to the BIS system.

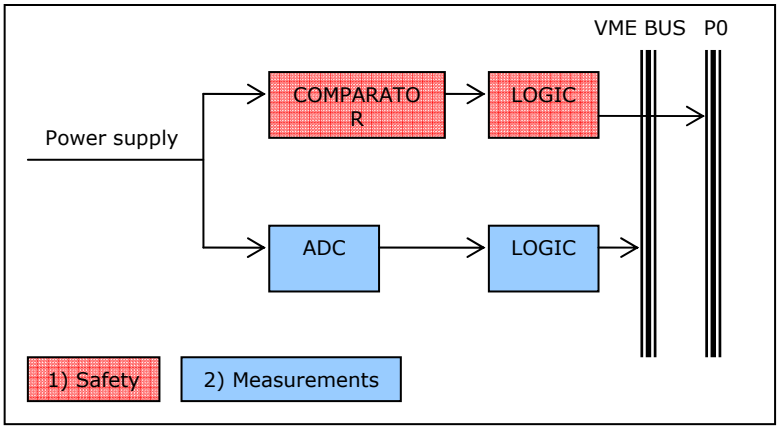
Name	Description	
UA	Unmaskable Left 'A'	
UB	Unmaskable Left 'B'	
MA	Maskable 'A'	
MB	Maskable 'B'	

3.3 MONITORING THE POWER SUPPLIES

The power supplies have to be monitored for safety purpose in case of a failure of one of the power supplies components.

Name	Description	Limit level
HV >	High Voltage higher	
HV <	High Voltage Lower	
I >	HV Current Higher	
I <	HV Current Lower	
+3V	3.3V Power supply	
+5V	5V Power supply	
±15V	±15V Power supply	

There are 2 distinct circuits to monitor them. Comparator with a fix threshold insures a fast response and a robust behaviour and the ADC reading permit to visualise the actual level and maybe take action before the drop of the voltage.



Safety monitoring

This function is made with comparators with hard wired setup (resistors) directly connected to the logic to send in case directly a fault further.

Measurements monitoring

In order to be able to visualize the actual voltage of all the supplies, a conversion to digital is performed and can be read through the VME bus.

3.4 VME INTERFACE

SLAVE MODE

This is the normal mode of the combiner inherited from the DAB64x card. The TC uses it to give access to the create CPU for login, post-mortem etc.

MASTER MODE

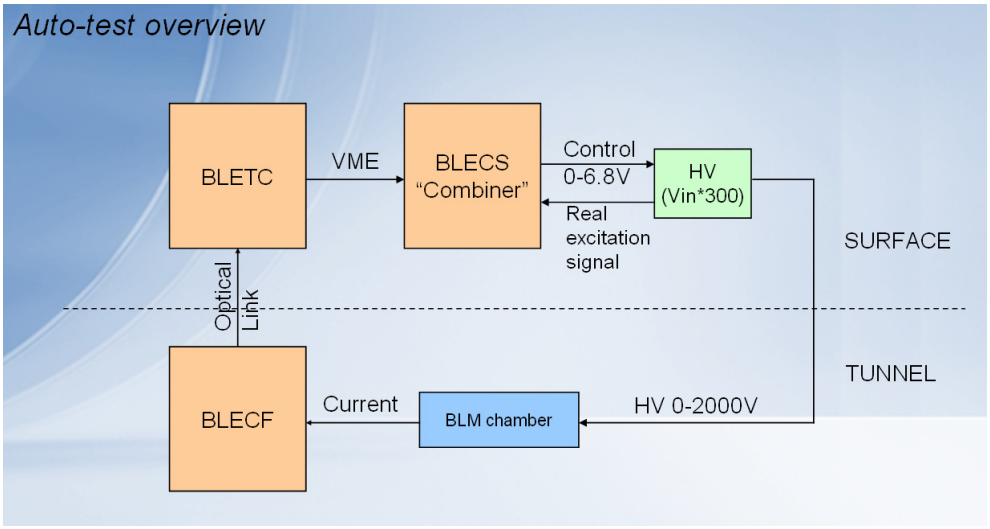
In this mode, it is the combiner which ask for bus mastering (DTB "Data Transfer Bus") in order to access to the TC and get measurement result when the test of the whole acquisition chain take place.

3.5 P2 CONNECTOR TABLE

Pin number	Name	Description
	UA in	Unmaskable Left 'A'
	UB in	Unmaskable Left 'B'
	MA in	Maskable 'A'
	MB in	Maskable 'B'
	UA out	Unmaskable Left 'A'
	UB out	Unmaskable Left 'B'
	MA out	Maskable 'A'
	MB out	Maskable 'B'
	HV1C	High voltage 1 command
	HV2C	High voltage 2 command
	HV1M	High voltage 1 monitor
	HV2M	High voltage 2 monitor
	BE0 in	Beam Energy Bit 0
	BE1 in	Beam Energy Bit 1
	BE2 in	Beam Energy Bit 2
	BE3 in	Beam Energy Bit 3
	BE4 in	Beam Energy Bit 4
	BE5 in	Beam Energy Bit 5
	BES in	Beam Energy Synch

3.6 AUTO-TEST OF THE BLM ACQUISITION CHAIN

The combiner checks if the whole chain is working by generating a modulation on the high voltage power supply of the chamber. This modulation passes through the multiple components of the system and is checked on the surface.



The control and acquisition chain is represented on the figure; the HT which is controlled by the combiner feed the chambers with voltage. Then the chamber generate current, the CFC card measure these values and transmit them to the TC card. The resulting running sums are then taken by the combiner through the VME.

There are 2 type of test :

1. Addition of a step on the high voltage
2. Addition of a low voltage modulation on the high voltage

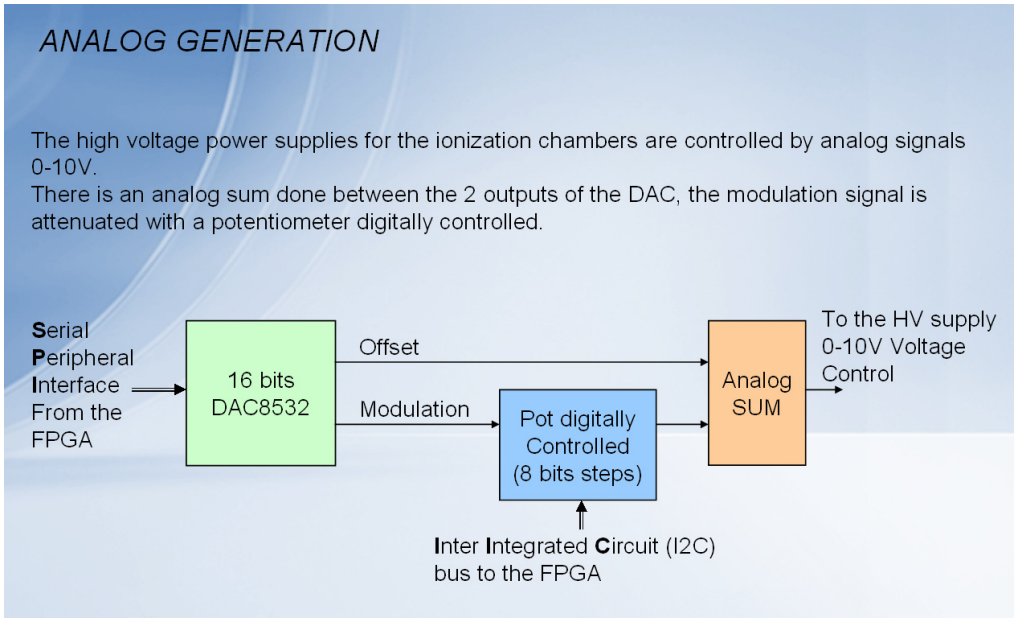
3.6.1 ADDITION OF A STEP ON THE HIGH VOLTAGE

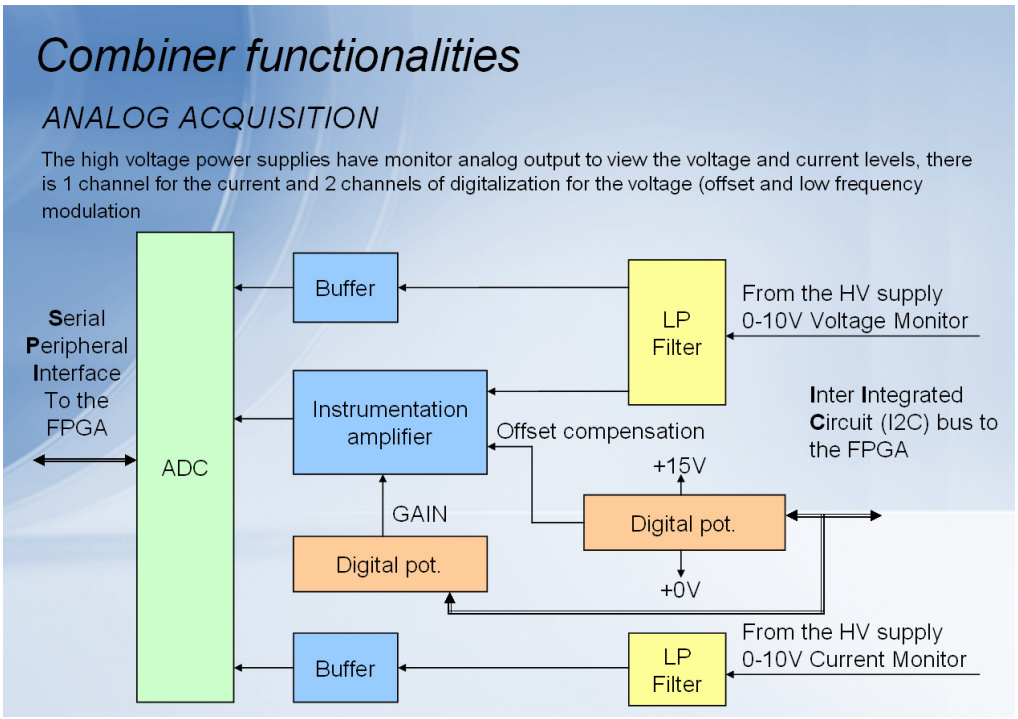
The high voltage will be increased in order to signal to the CFC card to start 3 types of functions :

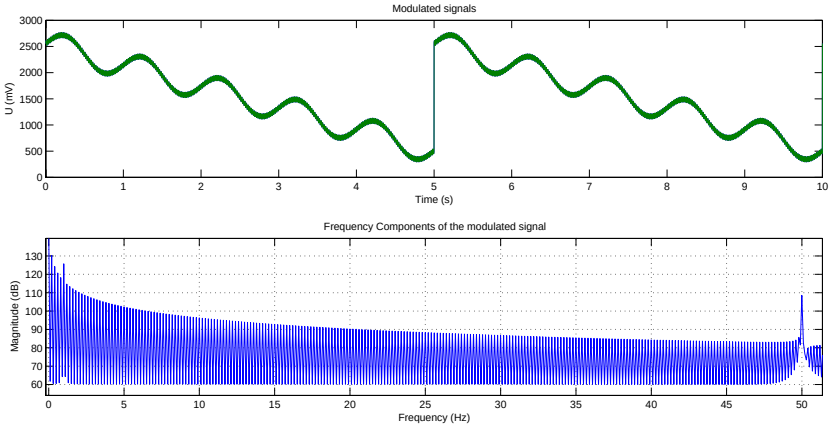
1. 10% ? highter to start a so called "Test_CFC". An 50pA current will be added to the initial current of the current compensation loop in order to check the hwhole cabling system.
2. 20% ? highter to start a so called "Reset_DAC". The compensation current will be set to 0. After this reset, the loop will be enable again to reach the correct value. This function previens an over compensation due to the beam.
3. 30% ? highter to start a so called "Reset_GOH". In some rare case, the pll of the GOH can be stuck if a SEU (Single Event Upset) occure. The only action for starting again the transmission on the optical fiber is to turn off the power supply of theis GOH and then on again.

3.6.2 ADDITION OF A LOW VOLTAGE MODULATION ON THE HIGH VOLTAGE

Initiate and realize the test of the cabling to check the entire acquisition chain from the high voltage supply to the TC.







The final ADC values readings and its low frequencies components

Self test through the Maximum Sums

If the modulation is enough slow, the maximum of the sums updated every seconde can be used to visualize the modulation. The information can be taken in the 40μs sum which is the smallest sum of the system.

4. POST MORTEM

The data organization in the post mortem memory is presented as below.

Each change in the state of flags (1 bit) or values (n bits) with an '*' or '**' trig one new record in the post mortem memory.

The normal state of the flags with an '**' is '1', when a problem occurs, the state change to '0' and this state is frozen until there is a read by the CPU. Even if one or more flags are frozen, the others can change there state and a new record in the post mortem memory will be done.

Timing info:

Turn number since last reset	32bits	
(Time Stamp	64bits)	UTC?

Beam Energy:

*Present Value	16bits	
CRC error reception channel A	32bits	from CTRV positive signal line
CRC error reception channel B	32bits	from CTRV complementary signal line

User Beam Permit:

**TC UnMaskable		1bit	from create Threshold Comparators
**TC Maskable		1bit	
**IN UnMaskable	'A'	1bit	from upper Combiner
**IN UnMaskable	'B'	1bit	
**IN Maskable	'A'	1bit	
**IN Maskable	'B'	1bit	
**OUT UnMaskable	'A'	1bit	to lower Combiner
**OUT UnMaskable	'B'	1bit	
**OUT Maskable	'A'	1bit	
**OUT Maskable	'B'	1bit	
*Beam info	'A'	1bit	from CIBUS
*Beam info	'B'	1bit	(Controls Interlocks Beam User Single) [ref]

Auto-test:

*Auto-test is pending	1bit
*Expert test is pending	1bit

HV (High Voltage):

**HV1 Voltage	1bit
**HV1 Current	1bit
**HV2 Voltage	1bit
**HV2 Current	1bit

LV (Low Voltage):

**LV Analog 5V	1bit	P0 power supplies for HV control & Auto-test
**LV Analog ±15V	1bit	
**LV Digital 3.3V	1bit	VME power supplies
**LV Digital 5V	1bit	
**LV Digital ±12V	1bit	

System level:

**System is operational	1bit

5. LOGIN

The data organization in the login memory is presented as below.

There are two type of login. Every second, the CPU will take the state of the hardware and the user beam permits.

Only after an auto-test, the CPU will be requested to upload the setup and result of the auto-test.

5.1 EVERY SECOND

System level:

System is operational	1bit	
System is under test	1bit	
User test pending	1bit	
Expert test pending	1bit	
Tests pending	5bits	bit4: System test, bit3: Consistency, bit2: BPBIS, bit1: HVRDAC, bit0: HVRGOH
System next test request	32bits	time in second remained before next test request
System next critical test	32bits	time in second remained before next critical test request
System Test requested	2bits	bit1: Beam permit away next dump (24 hours) bit0: Test requested (12 hours)

Active tests Overview at the moment:

The tests below with an 'S' are part of the system test that must be done within a certain time. The tests with '*' can be triggered independently of the system test. The timers are not modified when a test with '*' is triggered.

S *	T1: Consistency	1bit	Energy increase for Thresholds reading
S	T2: AutoTestAcqChain(Modulation)	1bit	Low frequency modulation test
S	T3: BILTC (Beam Inhibit Lines)	1bit	test of the lines between TC and BLECS
*	T4: BPBIS (Beam Permit to the LBIS)	1bit	BLECS - LHC Beam Interlock System
S	T5: HVTCFC (TEST CFC)	1bit	Activation TEST_CFC on the tunnel cards
*	T6: HVRDAC (DAC RESET)	1bit	Activation RST_DAC on the tunnel cards
*	T7: HVRGOH (GOH RESET)	1bit	Activation RST_GOH on the tunnel cards

Results of the last System test:

Time stamp when last test	32bits or 64bits
System test successful	1bit
Consistency successful	1bit
AutoTestAcqChain(Modulation)	1bit
BILTC (Beam Inhibit Lines)	1bit
HVTCFC (TEST CFC)	1bit

Timing info:

Turn number since last reset	32bits
(Time Stamp	64bits) UTC?

User Beam Permit:

TC	UnMaskable		1bit	from create Threshold comparators
TC	Maskable		1bit	
IN	UnMaskable	'A'	1bit	from upper Combiner
IN	UnMaskable	'B'	1bit	
IN	Maskable	'A'	1bit	
IN	Maskable	'B'	1bit	

OUT	UnMaskable	'A'	1bit	to lower Combiner
OUT	UnMaskable	'B'	1bit	
OUT	Maskable	'A'	1bit	
OUT	Maskable	'B'	1bit	
Beam info		'A'	1bit	from CIBUS
Beam info		'B'	1bit	(Controls Interlocks Beam User Single) [ref]

Beam Energy:

Actual Value	16bits	
CRC error reception channel A	32bits	from CTRV positive signal line
CRC error reception channel B	32bits	from CTRV complementary signal line

HV (High Voltage):

HV1 Voltage value	14bits	High tension power supply principal
HV1 Voltage Higher	1bit	
HV1 Voltage Lower	1bit	
HV1 Current value	14bits	
HV1 Current Higher	1bit	
HV1 Current Lower	1bit	
HV2 Voltage value	14bits	High tension power supply backup
HV2 Voltage Higher	1bit	
HV2 Voltage Lower	1bit	
HV2 Current value	14bits	
HV2 Current Higher	1bit	
HV2 Current Lower	1bit	

LV (Low Voltage):

LV Analog 5V	1bit	P0 power supply for Autotest only
LV Analog 5V Counter ripples	32bits	
LV Analog ±15V	1bit	P0 power supply for Autotest only
LV Analog ±15V Counter ripples	32bits	
LV Digital 3.3V	1bit	VME power supply
LV Digital 3.3V Counter ripples	32bits	
LV Digital 5V	1bit	VME power supply
LV Digital 5V Counter ripples	32bits	
LV Digital ±12V	1bit	VME power supply
LV Digital ±12V Counter ripples	32bits	

TBC Components Diagnostic:

Memory ROM	1bit
Memory flash	1bit
Analog digital converter answering	1bit
Front panel leds answering	1bit
Digital potentiometer 0	1bit
Digital potentiometer 1	1bit

5.2 EVERY REQUEST BY THE HARDWARE

The informations contained in this section are changing only when an Auto-test or an Expert test occurs. In this context, there is no need to log them every second. The way used to inform the CPU of a need for uploading data is the following. There is a counter which is incremented by one each time the hardware ask for a new read.

T5 to T7: High voltage tests **setup**:

HVTCFC	(TEST CFC)	16bit	HV Level applied in case this test
HVRDAC	(DAC RESET)	16bit	HV Level applied in case this test
HVRGOH	(GOH RESET)	16bit	HV Level applied in case this test

T3: BILTC (Beam Inhibit Lines)**setup**:

TC boards map	16bits	'1' when present otherwise '0'

T3: BILTC (Beam Inhibit Lines)**result**:

BILTC last result	1bit	'1' if passed
TC boards test result	16bits	'1' when present otherwise '0'

T2: Auto test **setup**:

Modulation amplitude	16bits	at the output of the DAC (10V max)
Modulation attenuation 1	8bits	setup of the digital potentiometer 1
Modulation attenuation 2	8bits	setup of the digital potentiometer 2
Offset voltage	16bits	at the output of the DAC (10V max)
Modulation measurement multiplication	8bits	setup of the digital potentiometer
Modulation measurement offset correction	8bits	setup of the digital potentiometer

Channel 1 setup:

Masked	1bit
Unconnected	1bit
Amplitude min	14bits
Amplitude max	14bits
Phase min	16bits
Phase max	16bits

…

Channel 256 setup:

Masked	1bit
Unconnected	1bit
Amplitude min	14bits
Amplitude max	14bits
Phase min	16bits
Phase max	16bits

T2: Auto test **results**:

Time stamp when last test	32bits or 64bits
Time stamp next test	32bits or 64bits
Auto-test is pending	1bit
Expert test is pending	1bit
Test successful	1bit
Number of tested TC	5bits
Number of tested channels	9bits
TC pos1 passed/failed	1bit
TC pos2 passed/failed	1bit
…	
TC pos16 passed/failed	1bit

Channel 1 result:

Passed/failed	1bit
Amplitude	14bits
phase	16bits
free	1bit

…

Channel 256 result:

Passed/failed	1bit
Amplitude	14bits
phase	16bits
free	1bit

6. ACCESS BY THE CREATE CPU