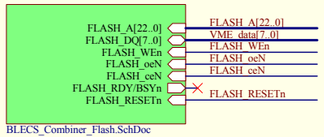
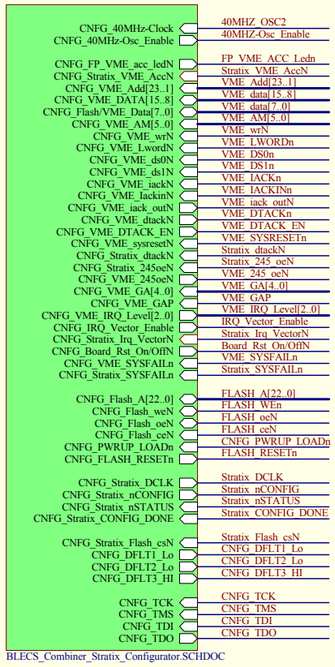
Flash



BLECS_Combiner_Flash.SchDoc

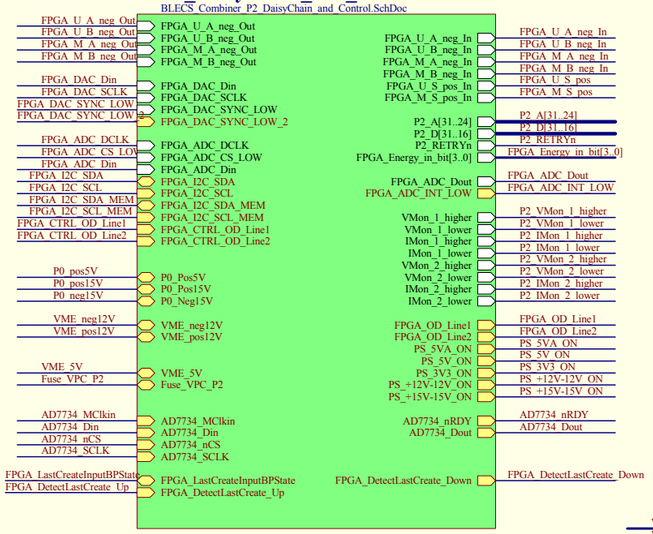
Stratix_Configurator



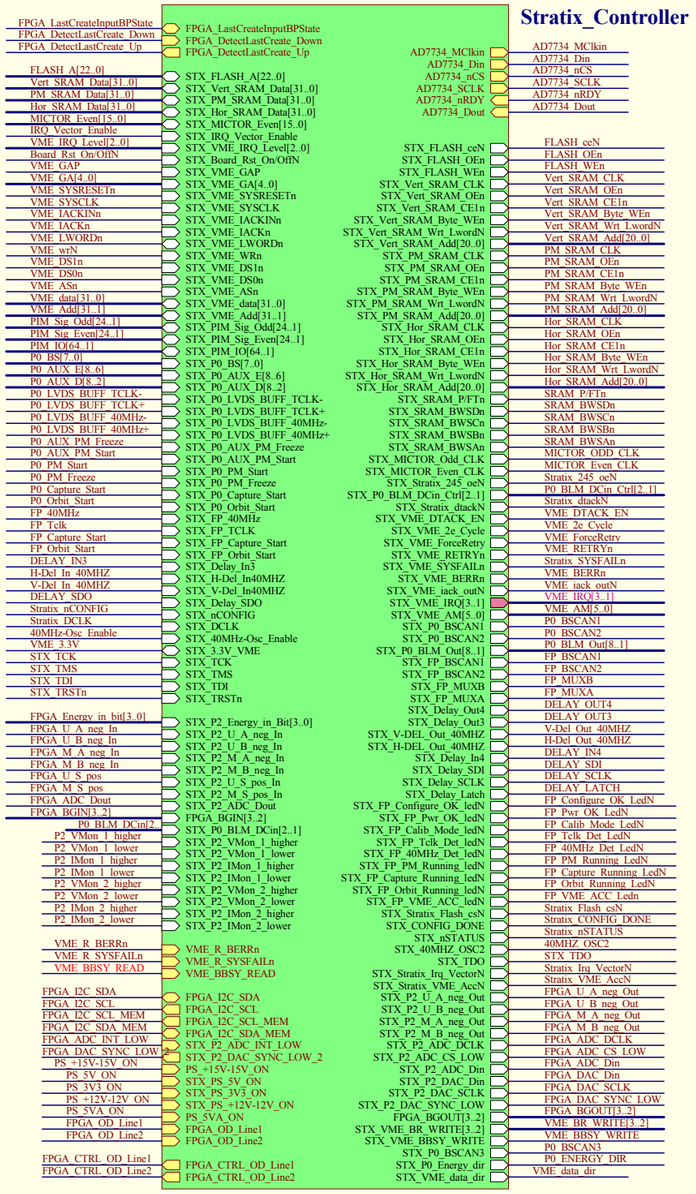
BLECS_Combiner_Stratix_Configurator.SCHDOC

P2_DaisyChain_and_Control

BLECS_Combiner_P2_DaisyChain_and_Control.SchDoc

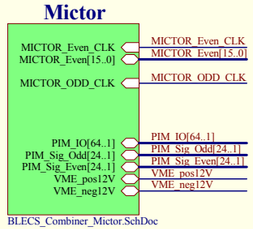


Stratix_Controller



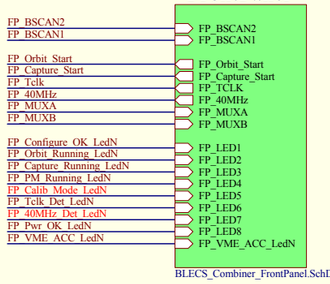
BLECS_Combiner_Stratix_Controller.SCHDOC

Mictor



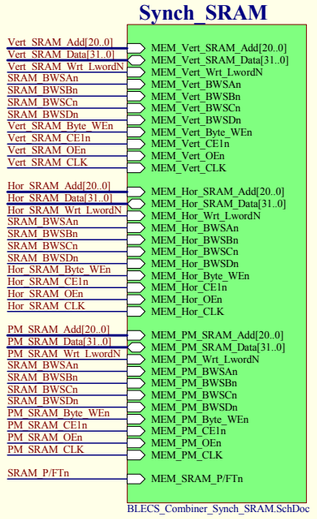
BLECS_Combiner_Mictor.SchDoc

FrontPanel



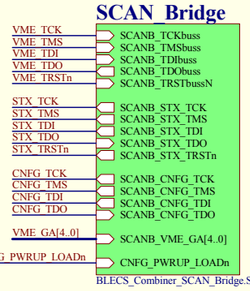
BLECS_Combiner_FrontPanel.SchDoc

Synch_SRAM



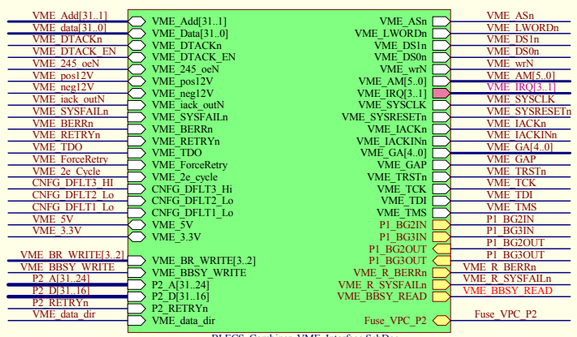
BLECS_Combiner_Synch_SRAM.SchDoc

SCAN_Bridge



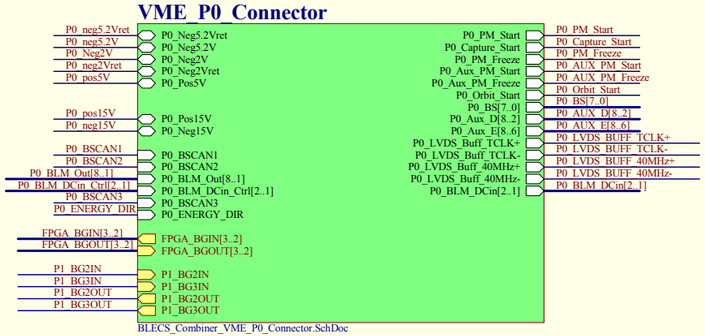
BLECS_Combiner_SCAN_Bridge.SchDoc

VME_Interface



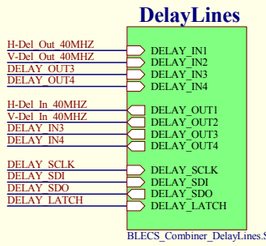
BLECS_Combiner_VME_Interface.SchDoc

VME_P0_Connector



BLECS_Combiner_VME_P0_Connector.SchDoc

DelayLines



BLECS_Combiner_DelayLines.SchDoc

BLECS MODULE

Revision				
3	CERN EDMS: EDA-01660		*CERN* based on DAB64x by TRIUMF	Cannot open file TRIUMF.BMP
	Sheet #: 1 of 12	Size: C		
	Drawn by: J. Emery	Date: 05/12/2007		

File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combiner_Module.SchDoc

U_ : Unmaskable / M_ : Maskable / _A_ : ChannelA / _B_ : ChannelB

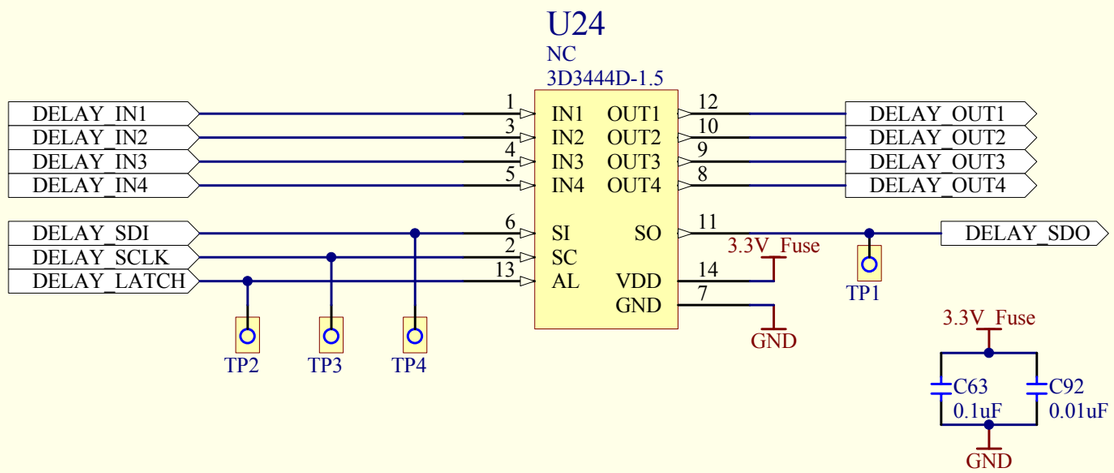
To determine if the board is the last one before the CIBUS

To Send/Receive the state of the BP on the last BLECS before the CIBU

DAC CHECK

ADC CHECK

Title	BLECS: VME P2 CONTROLS
Size	D
Number	CERN EDMS: EDA-01660
	J. Emery
Revision	3
Date:	05/12/2007
Sheet 2 of 12	
File:	C:\LOCAL_DESIGN\...\BLECS_Combined_Top_Bottom_Chain_and_Control.SchDoc



BLECS: Delay Lines

Revision			
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	Sheet #: 3 of 12	Size: A	
	Drawn by: J. Emery	Date: 05/12/2007	
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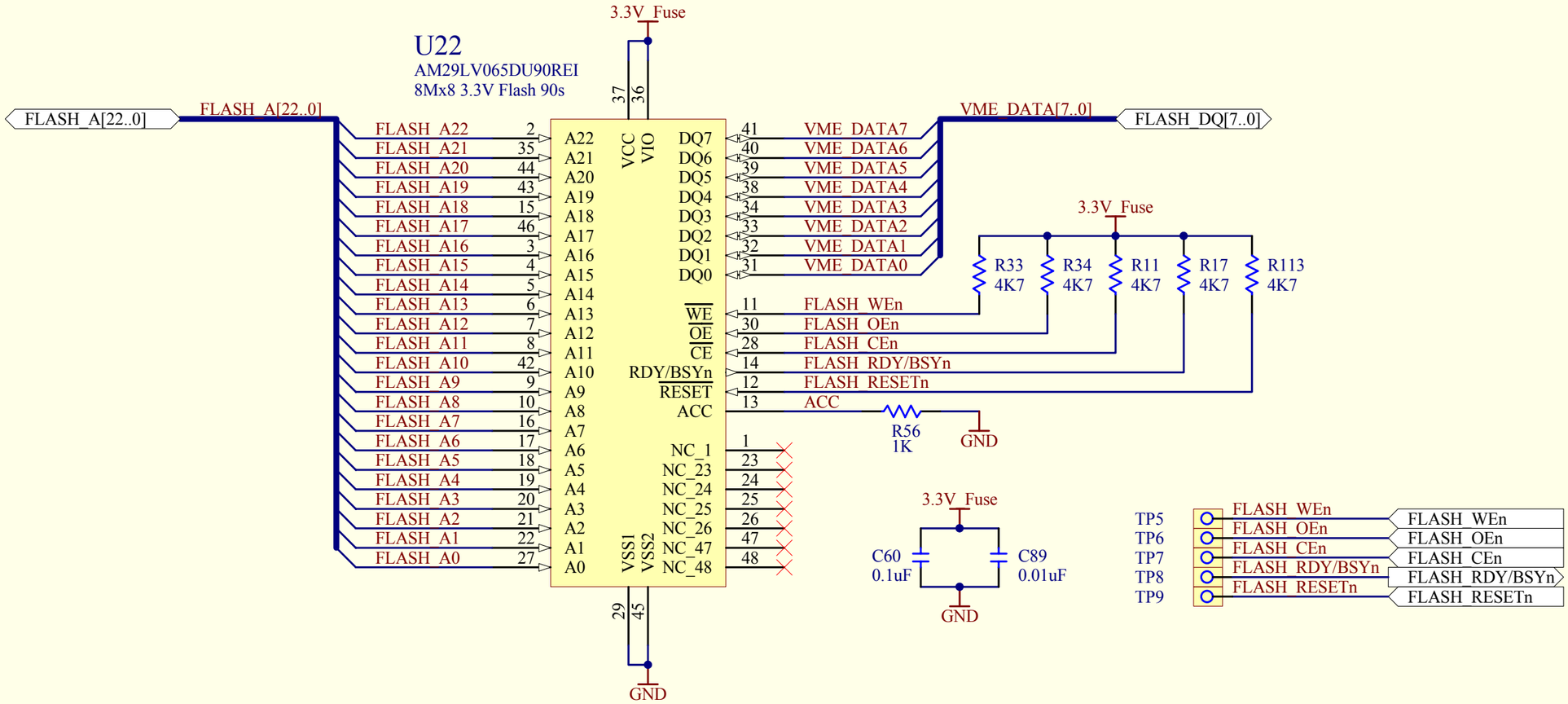
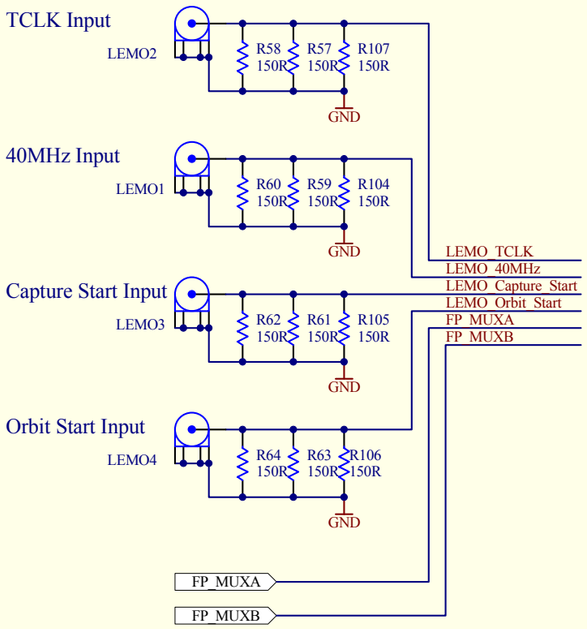
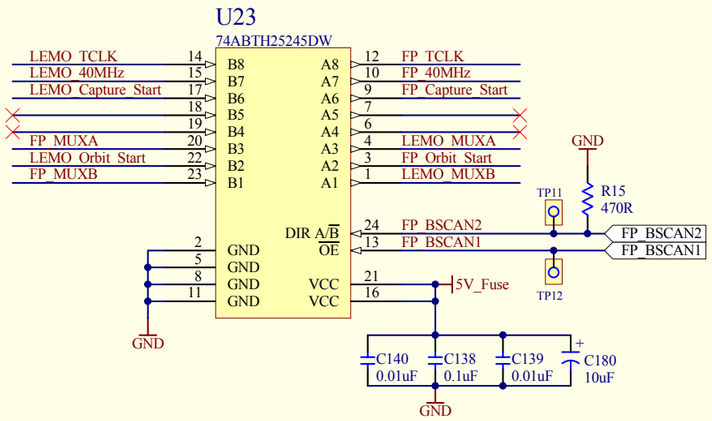
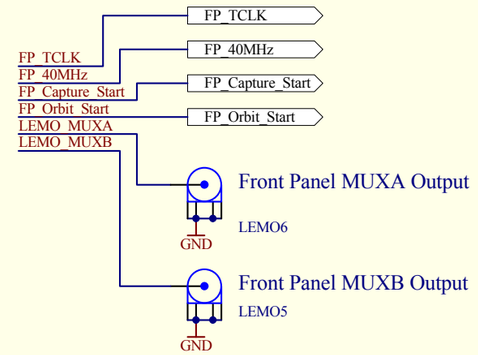


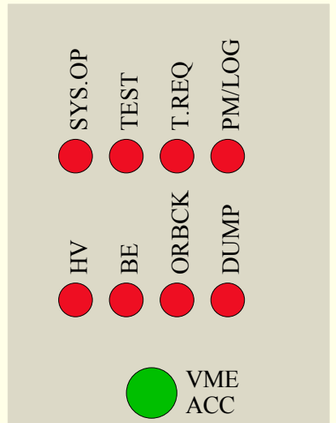
BLECS: Flash Configuration Memory

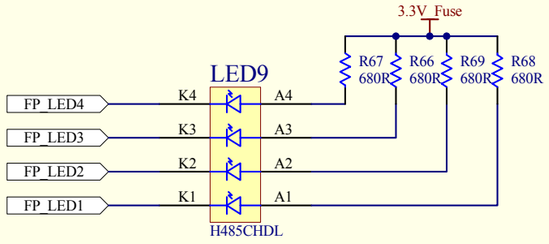
Revision 3	CERN EDMS: EDA-01660		*CERN* based on DAB64x by TRIUMF
	Sheet #: 4 of 12	Size: A	
	Drawn by: J. Emery	Date: 05/12/2007	
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combiner_Flash.SchDoc			

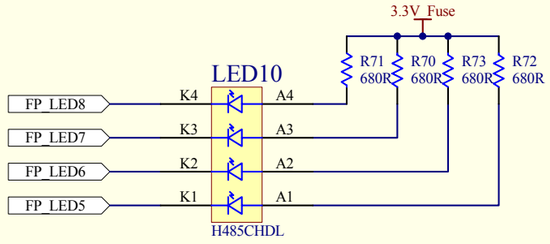


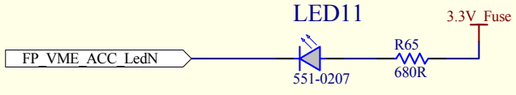






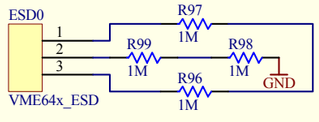


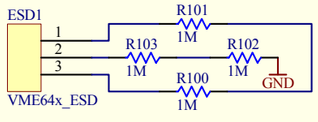




VME Access

ESD Front Panel Discharge Resistors





BLECS: Front Panel Display and Signal I/O

Revision			
3	CERN EDMS: EDA-01660		*CERN* based on DAB64x by TRIUMF
	Sheet #: 5 of 12	Size: B	
	Drawn by: J. Emery	Date: 05/12/2007	

File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combine

J3

TP131 — MICTOR_Even_CLK

TP132 — MICTOR_ODD_CLK

			1	HP_+5VDC	HP_SCL	2	
			3	HP_GND	HP_SDA	4	
		MICTOR_Even_CLK	5	EvenPod_CLK	OddPod_CLK	6	MICTOR_ODD_CLK
TP133		MICTOR_Even15	7	EvenPod_D15	OddPod_D15	8	PIM_IO16
TP134		MICTOR_Even14	9	EvenPod_D14	OddPod_D14	10	PIM_IO15
TP135		MICTOR_Even13	11	EvenPod_D13	OddPod_D13	12	PIM_IO14
TP136		MICTOR_Even12	13	EvenPod_D12	OddPod_D12	14	PIM_IO13
TP137		MICTOR_Even11	15	EvenPod_D11	OddPod_D11	16	PIM_IO12
TP138		MICTOR_Even10	17	EvenPod_D10	OddPod_D10	18	PIM_IO11
TP139		MICTOR_Even9	19	EvenPod_D9	OddPod_D9	20	PIM_IO10
TP140		MICTOR_Even8	21	EvenPod_D8	OddPod_D8	22	PIM_IO9
TP141		MICTOR_Even7	23	EvenPod_D7	OddPod_D7	24	PIM_IO8
TP142		MICTOR_Even6	25	EvenPod_D6	OddPod_D6	26	PIM_IO7
TP143		MICTOR_Even5	27	EvenPod_D5	OddPod_D5	28	PIM_IO6
TP144		MICTOR_Even4	29	EvenPod_D4	OddPod_D4	30	PIM_IO5
TP145		MICTOR_Even3	31	EvenPod_D3	OddPod_D3	32	PIM_IO4
TP146		MICTOR_Even2	33	EvenPod_D2	OddPod_D2	34	PIM_IO3
TP147		MICTOR_Even1	35	EvenPod_D1	OddPod_D1	36	PIM_IO2
TP148		MICTOR_Even0	37	EvenPod_D0	OddPod_D0	38	PIM_IO1

NC

MICTOR 38 pin HP Probe (2-767004-2)

MICTOR_Even[15..0] — MICTOR_Even[15..0]

Jn0

Molex_71439-0164

TP149	PIM_Sig_Odd1	1	Signal_p1	pos12V	2	VME_pos12V		
TP152	PIM_Sig_Odd2	3	Signal_p3	Signal_p4	4	PIM_Sig_Even1		
	5V_Fuse	5	5V_p5	Signal_p6	6	PIM_Sig_Even2	TP153	
TP159	PIM_Sig_Odd3	7	Signal_p7	Signal_p8	8	PIM_Sig_Even3	TP156	
TP163	PIM_Sig_Odd4	9	Signal_p9	3.3V_p10	10	3.3V_Fuse	TP160	
TP166	PIM_Sig_Odd5	11	Signal_p11	Signal_p12	12	PIM_Sig_Even4		
	GND	13	GND_p13	Signal_p14	14	PIM_Sig_Even5	TP167	
TP173	PIM_Sig_Odd6	15	Signal_p15	Signal_p16	16	PIM_Sig_Even6	TP170	
TP177	PIM_Sig_Odd7	17	Signal_p17	GND_p18	18	GND	TP174	
TP180	PIM_Sig_Odd8	19	Signal_p19	Signal_p20	20	PIM_Sig_Even7		
	5V_Fuse	21	5V_p21	Signal_p22	22	PIM_Sig_Even8	TP181	
	PIM_Sig_Odd9	23	Signal_p23	Signal_p24	24	PIM_Sig_Even9	TP184	
TP187	PIM_Sig_Odd10	25	Signal_p25	3.3V_p26	26	3.3V_Fuse	TP188	
TP191	PIM_Sig_Odd11	27	Signal_p27	Signal_p28	28	PIM_Sig_Even10		
TP194	GND	29	GND_p29	Signal_p30	30	PIM_Sig_Even11	TP195	
	PIM_Sig_Odd12	31	Signal_p31	Signal_p32	32	PIM_Sig_Even12	TP198	
TP201	PIM_Sig_Odd13	33	Signal_p33	GND_p34	34	GND	TP202	
TP205	PIM_Sig_Odd14	35	SIgnal_p35	Signal_p36	36	PIM_Sig_Even13		
TP208	5V_Fuse	37	5V_p37	Signal_p38	38	PIM_Sig_Even14	TP209	
	PIM_Sig_Odd15	39	Signal_p39	Signal_p40	40	PIM_Sig_Even15	TP212	
TP215	PIM_Sig_Odd16	41	Signal_p41	3.3V_p42	42	3.3V_Fuse	TP216	3.3V_Fuse
TP219	PIM_Sig_Odd17	43	Signal_p43	Signal_p44	44	PIM_Sig_Even16		
TP222	GND	45	GND_p45	Signal_p46	46	PIM_Sig_Even17	TP223	
	PIM_Sig_Odd18	47	Signal_p47	Signal_p48	48	PIM_Sig_Even18	TP226	
TP229	PIM_Sig_Odd19	49	Signal_p49	GND_p50	50	GND	TP230	GND
TP233	PIM_Sig_Odd20	51	Signal_p51	Signal_p52	52	PIM_Sig_Even19		
TP236	5V_Fuse	53	5V_p53	Signal_p54	54	PIM_Sig_Even20	TP237	
5V_Fuse	PIM_Sig_Odd21	55	Signal_p55	Signal_p56	56	PIM_Sig_Even21	TP240	
TP243	PIM_Sig_Odd22	57	Signal_p57	3.3V_p58	58	3.3V_Fuse	TP244	
TP247	PIM_Sig_Odd23	59	Signal_p59	Signal_p60	60	PIM_Sig_Even22		
TP250	VME_neg12V	61	neg12V	Signal_p62	62	PIM_Sig_Even23	TP251	
	PIM_Sig_Odd24	63	Signal_p63	Signal_p64	64	PIM_Sig_Even24	TP254	
TP257							TP258	

Jn4

Molex_71439-0164

TP150	PIM_IO1	1	IO1	IO2	2	PIM_IO2		
TP154	PIM_IO3	3	IO3	IO4	4	PIM_IO4	TP151	
TP157	PIM_IO5	5	IO5	IO6	6	PIM_IO6	TP155	
TP161	PIM_IO7	7	IO7	IO8	8	PIM_IO8	TP158	
TP164	PIM_IO9	9	IO9	IO10	10	PIM_IO10	TP162	
TP168	PIM_IO11	11	IO11	IO12	12	PIM_IO12	TP165	
TP171	PIM_IO13	13	IO13	IO14	14	PIM_IO14	TP169	
TP175	PIM_IO15	15	IO15	IO16	16	PIM_IO16	TP172	
TP178	PIM_IO17	17	IO17	IO18	18	PIM_IO18	TP176	
TP182	PIM_IO19	19	IO19	IO20	20	PIM_IO20	TP179	
TP185	PIM_IO21	21	IO21	IO22	22	PIM_IO22	TP183	
TP189	PIM_IO23	23	IO23	IO24	24	PIM_IO24	TP186	
TP192	PIM_IO25	25	IO25	IO26	26	PIM_IO26	TP190	
TP196	PIM_IO27	27	IO27	IO28	28	PIM_IO28	TP193	
TP199	PIM_IO29	29	IO29	IO30	30	PIM_IO30	TP197	
TP203	PIM_IO31	31	IO31	IO32	32	PIM_IO32	TP200	
TP206	PIM_IO33	33	IO33	IO34	34	PIM_IO34	TP204	
TP210	PIM_IO35	35	IO35	IO36	36	PIM_IO36	TP207	
TP213	PIM_IO37	37	IO37	IO38	38	PIM_IO38	TP211	
TP217	PIM_IO39	39	IO39	IO40	40	PIM_IO40	TP214	
TP220	PIM_IO41	41	IO41	IO42	42	PIM_IO42	TP218	
TP224	PIM_IO43	43	IO43	IO44	44	PIM_IO44	TP221	
TP227	PIM_IO45	45	IO45	IO46	46	PIM_IO46	TP225	
TP231	PIM_IO47	47	IO47	IO48	48	PIM_IO48	TP228	
TP234	PIM_IO49	49	IO49	IO50	50	PIM_IO50	TP232	
TP238	PIM_IO51	51	IO51	IO52	52	PIM_IO52	TP235	
TP241	PIM_IO53	53	IO53	IO54	54	PIM_IO54	TP239	
TP245	PIM_IO55	55	IO55	IO56	56	PIM_IO56	TP242	
TP248	PIM_IO57	57	IO57	IO58	58	PIM_IO58	TP246	
TP252	PIM_IO59	59	IO59	IO60	60	PIM_IO60	TP249	
TP255	PIM_IO61	61	IO61	IO62	62	PIM_IO62	TP253	
TP259	PIM_IO63	63	IO63	IO64	64	PIM_IO64	TP256	
							TP260	

VME_pos12V — VME_pos12V

VME_neg12V — VME_neg12V

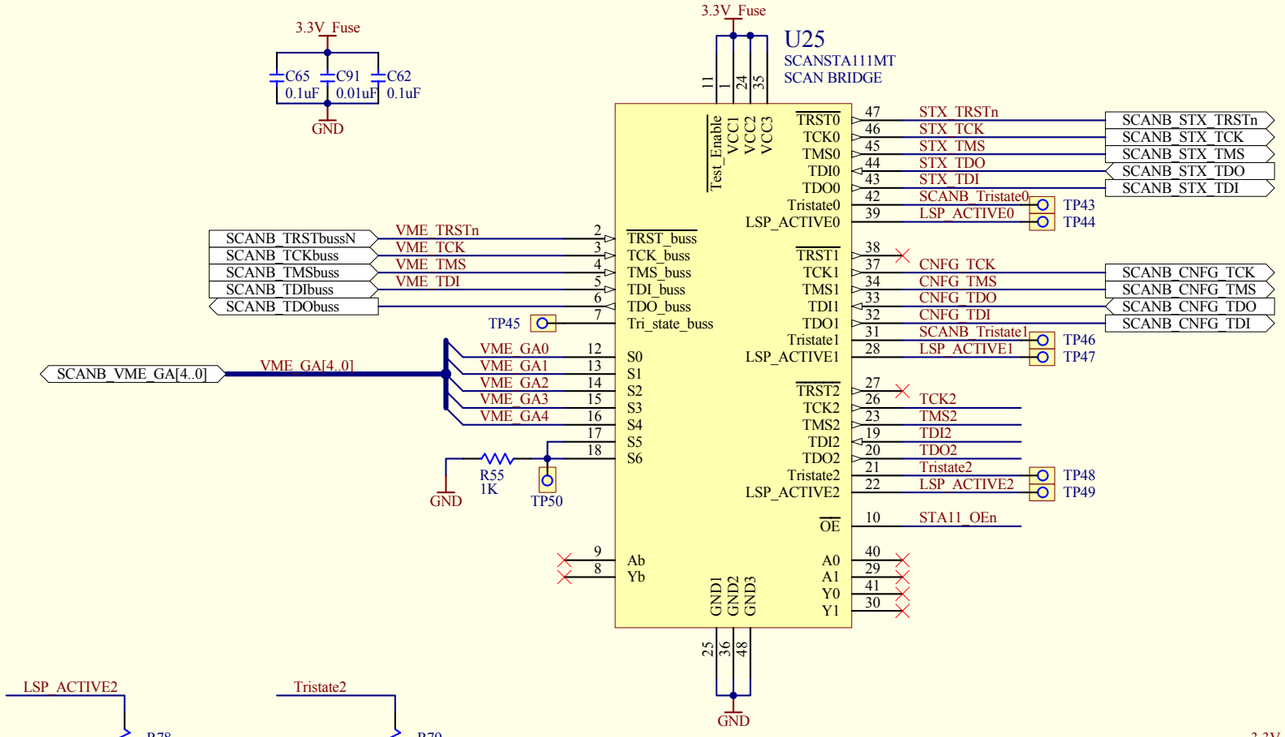
PIM_IO[64..1] — PIM_IO[64..1]

PIM_Sig_Even[24..1] — PIM_Sig_Even[24..1]

PIM_Sig_Odd[24..1] — PIM_Sig_Odd[24..1]

BLECS: MICTOR Connector / PIM Mezzanine Connectors

Revision 3	CERN EDMS: EDA-01660		CERN based on DAB64x by TRIUMF
	Sheet #: 6 of 12	Size: A	
	Drawn by: J. Emery	Date: 05/12/2007	
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combiner_Mictor.SchDoc			



BLECS: JTAG Interface / Scanbridge

Revision 3	CERN EDMS: EDA-01660		CERN based on DAB64x by TRIUMF
	Sheet #: 7 of 12	Size: B	
	Drawn by: J. Emery	Date: 05/12/2007	
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics.SchDoc			BLECS_Combine

U100A
EPM3256ATC144-10

Stratix_dtackN	1	Stratix_dtackN
VME_Add17	2	VME_Add[17]
GND	3	GND
CNFG_TDI	4	TDI
FP_VME_acc_ledN	5	VME_acc_ledN
CNFG_PWRUP_LOADn	6	CNFG_PWRUP_LOADn
40MHz-Osc_Enable	7	40MHz-Osc_Enable
Stratix_Flash_csN	8	Stratix_Flash_csN
Stratix_245_oeN	9	Stratix_245_oeN
VME_IRQ_Level0	10	VME_IRQ_Level[0]
VME_IRQ_Level2	11	VME_IRQ_Level[2]
VME_Add19	12	VME_Add[19]
GND	13	GND
VME_IRQ_Level1	14	VME_IRQ_Level[1]
Stratix_Irq_VectorN	15	Stratix_Irq_VectorN
Flash_A21	16	Flash_add[21]
GND	17	GND
Flash_A22	18	Flash_add[22]
Board_Rst_On/OffN	19	Board_Rst_On/OffN
CNFG_TMS	20	TMS
VME_Add21	21	VME_Add[21]
VME_Add22	22	VME_Add[22]
VME_Add23	23	VME_Add[23]
3.3V_Fuse	24	VCCIO
Stratix_VME_AccN	25	Stratix_VME_AccN
GND	26	GND
VME_AM1	27	VME_AM[1]
Stratix_nSTATUS	28	Stratix_nSTATUS
Stratix_nCONFIG	29	Stratix_nCONFIG
Stratix_DCLK	30	Stratix_DCLK
VME_Add3	31	VME_Add[3]
VME_Add4	32	VME_Add[4]
GND	33	GND
VME_AM0	34	VME_AM[0]
IRQ_Vector_Enable	35	IRQ_Vector_Enable
VME_AM2	36	VME_AM[2]

U100B
EPM3256ATC144-10

VME_Add16	37	VME_Add[16]
CNFG_DFLT3_Hi	38	CNFG_DFLT3_HI
CNFG_DFLT2_Lo	39	CNFG_DFLT2_Lo
VME_wrN	40	VME_wrN
CNFG_DFLT1_Lo	41	CNFG_DFLT1_Lo
VME_LwordN	42	VME_LwordN
Stratix_SYSFAILn	43	Stratix_SYSFAILn
VME_ds0N	44	VME_ds0N
VME_ds1N	45	VME_ds1N
VME_Add20	46	VME_Add[20]
VME_DATA9	47	VME_Data[9]
VME_DATA4	48	Flash/VME_Data[4]
VME_AM4	49	VME_AM[4]
3.3V_Fuse	50	VCCIO
3.3V_Fuse	51	VCCINT
GND	52	GND
VME_DATA12	53	VME_Data[12]
VME_DATA1	54	Flash/VME_Data[1]
VME_Add15	55	VME_Add[15]
VME_Add14	56	VME_Add[14]
GND	57	GND
3.3V_Fuse	58	VCCINT
GND	59	GND
VME_Add13	60	VME_Add[13]
VME_Add12	61	VME_Add[12]
VME_Add11	62	VME_Add[11]
VME_Add10	63	VME_Add[10]
GND	64	GND
VME_Add9	65	VME_Add[9]
VME_DATA3	66	Flash/VME_Data[3]
VME_Add8	67	VME_Add[8]
VME_Add7	68	VME_Add[7]
VME_Add6	69	VME_Add[6]
VME_Add5	70	VME_Add[5]
VME_DATA7	71	Flash/VME_Data[7]
VME_DATA6	72	Flash/VME_Data[6]

U100C
EPM3256ATC144-10

3.3V_Fuse	73	VCCIO
VME_Add2	74	VME_Add[2]
VME_AM5	75	VME_AM[5]
3.3V_Fuse	76	VCCIO
GND	77	GND
VME_Add1	78	VME_Add[1]
VME_IackN	79	VME_IackN
VME_IackinN	80	VME_IackinN
VME_iack_outN	81	VME_iackoutN
VME_245_oeN	82	VME_245_oeN
VME_dtackN	83	VME_dtackN
VME_SYSFAILn	84	VME_SYSFAILn
GND	85	GND
VME_DTACK_EN	86	VME_DTACK_EN
Flash_A0	87	Flash_add[0]
Flash_ceN	88	Flash_csN
CNFG_TCK	89	TCK
VME_DATA14	90	VME_Data[14]
Flash_oeN	91	Flash_oeN
VME_DATA5	92	Flash/VME_Data[5]
VME_DATA15	93	VME_Data[15]
GND	94	GND
3.3V_Fuse	95	VCCIO
VME_DATA13	96	VME_Data[13]
VME_AM3	97	VME_AM[3]
VME_DATA0	98	Flash/VME_Data[0]
VME_DATA8	99	VME_Data[8]
VME_DATA2	100	Flash/VME_Data[2]
VME_DATA11	101	VME_Data[11]
VME_DATA10	102	VME_Data[10]
VME_GA4	103	VME_GA[4]
CNFG_TDO	104	TDO
GND	105	GND
Flash_A10	106	Flash_add[10]
Flash_A19	107	Flash_add[19]
VME_GA3	108	VME_GA[3]

U100D
EPM3256ATC144-10

Flash_A20	109	Flash_add[20]
Flash_A17	110	Flash_add[17]
VME_Add18	111	VME_Add[18]
Flash_A16	112	Flash_add[16]
Flash_A15	113	Flash_add[15]
GND	114	GND
3.3V_Fuse	115	VCCIO
Flash_A14	116	Flash_add[14]
Flash_A13	117	Flash_add[13]
Flash_A12	118	Flash_add[12]
FLASH_RESETn	119	FLASH_RESETn
VME_GA2	120	VME_GA[2]
VME_GA1	121	VME_GA[1]
VME_GA0	122	VME_GA[0]
3.3V_Fuse	123	VCCINT
GND	124	GND
40MHZ_OSC2	125	40MHZ-Clock
Stratix_CONFIG_DONE	126	Stratix_CONF_DONE
VME_sysresetN	127	VME_sysresetN
VME_GAP	128	VME_GAP
GND	129	GND
3.3V_Fuse	130	VCCINT
Flash_A11	131	Flash_add[11]
Flash_A9	132	Flash_add[9]
Flash_A8	133	Flash_add[8]
Flash_weN	134	Flash_weN
GND	135	GND
Flash_A18	136	Flash_add[18]
Flash_A7	137	Flash_add[7]
Flash_A6	138	Flash_add[6]
Flash_A5	139	Flash_add[5]
Flash_A4	140	Flash_add[4]
Flash_A3	141	Flash_add[3]
Flash_A2	142	Flash_add[2]
Flash_A1	143	Flash_add[1]
3.3V_Fuse	144	VCCIO

TP52

3.3V_Fuse

C141 0.001uF C142 0.001uF C143 0.001uF C144 0.001uF C145 0.001uF C146 0.001uF C147 0.001uF C148 0.001uF C172 0.001uF

GND

3.3V_Fuse

C68 0.1uF C70 0.1uF C71 0.1uF C72 0.1uF C73 0.1uF C74 0.1uF C75 0.1uF C77 0.1uF C173 0.1uF

GND

VME Interface

CNFG_VME_Add[23..1]	VME_Add[23..1]
CNFG_VME_DATA[15..8]	VME_DATA[15..8]
CNFG_Flash/VME_Data[7..0]	VME_DATA[7..0]
CNFG_VME_AM[5..0]	VME_AM[5..0]
CNFG_VME_wrN	VME_wrN
CNFG_VME_LwordN	VME_lwordN
CNFG_VME_ds0N	VME_ds0N
CNFG_VME_ds1N	VME_ds1N
CNFG_VME_245oeN	VME_245_oeN
CNFG_VME_dtackN	VME_dtackN
CNFG_VME_DTACK_EN	VME_DTACK_EN
CNFG_VME_IRQ_Level[2..0]	VME_IRQ_Level[2..0]
CNFG_VME_iackN	VME_iackN
CNFG_VME_IackinN	VME_iackinN
CNFG_VME_iack_outN	VME_iack_outN
CNFG_Stratix_Irq_VectorN	Stratix_Irq_VectorN
CNFG_Stratix_VME_AccN	Stratix_VME_AccN
CNFG_VME_sysresetN	VME_sysresetN
CNFG_FP_VME_acc_ledN	FP_VME_acc_ledN
CNFG_Board_Rst_On/OffN	Board_Rst_On/OffN
CNFG_VME_GA[4..0]	VME_GA[4..0]
CNFG_VME_GAP	VME_GAP
CNFG_Stratix_Flash_csN	Stratix_Flash_csN
CNFG_Stratix_dtackN	Stratix_dtackN
CNFG_Stratix_245oeN	Stratix_245_oeN
CNFG_IRQ_Vector_Enable	IRQ_Vector_Enable
CNFG_VME_SYSFAILn	VME_SYSFAILn
CNFG_Stratix_SYSFAILn	Stratix_SYSFAILn

JTAG/Boundary Scan

CNFG_TCK	CNFG_TCK
CNFG_TMS	CNFG_TMS
CNFG_TDI	CNFG_TDI
CNFG_TDO	CNFG_TDO
CNFG_DFLT2_Lo	CNFG_DFLT2_Lo
CNFG_DFLT1_Lo	CNFG_DFLT1_Lo
CNFG_DFLT3_HI	CNFG_DFLT3_Hi

Stratix Configuration

CNFG_40MHz-Osc_Enable	40MHZ-Osc_Enable
CNFG_40MHz-Clock	40MHZ_OSC2
CNFG_Stratix_DCLK	Stratix_DCLK
CNFG_Stratix_nCONFIG	Stratix_nCONFIG
CNFG_Stratix_nSTATUS	Stratix_nSTATUS
CNFG_Stratix_CONFIG_DONE	Stratix_CONFIG_DONE
CNFG_PWRUP_LOADn	CNFG_PWRUP_LOADn

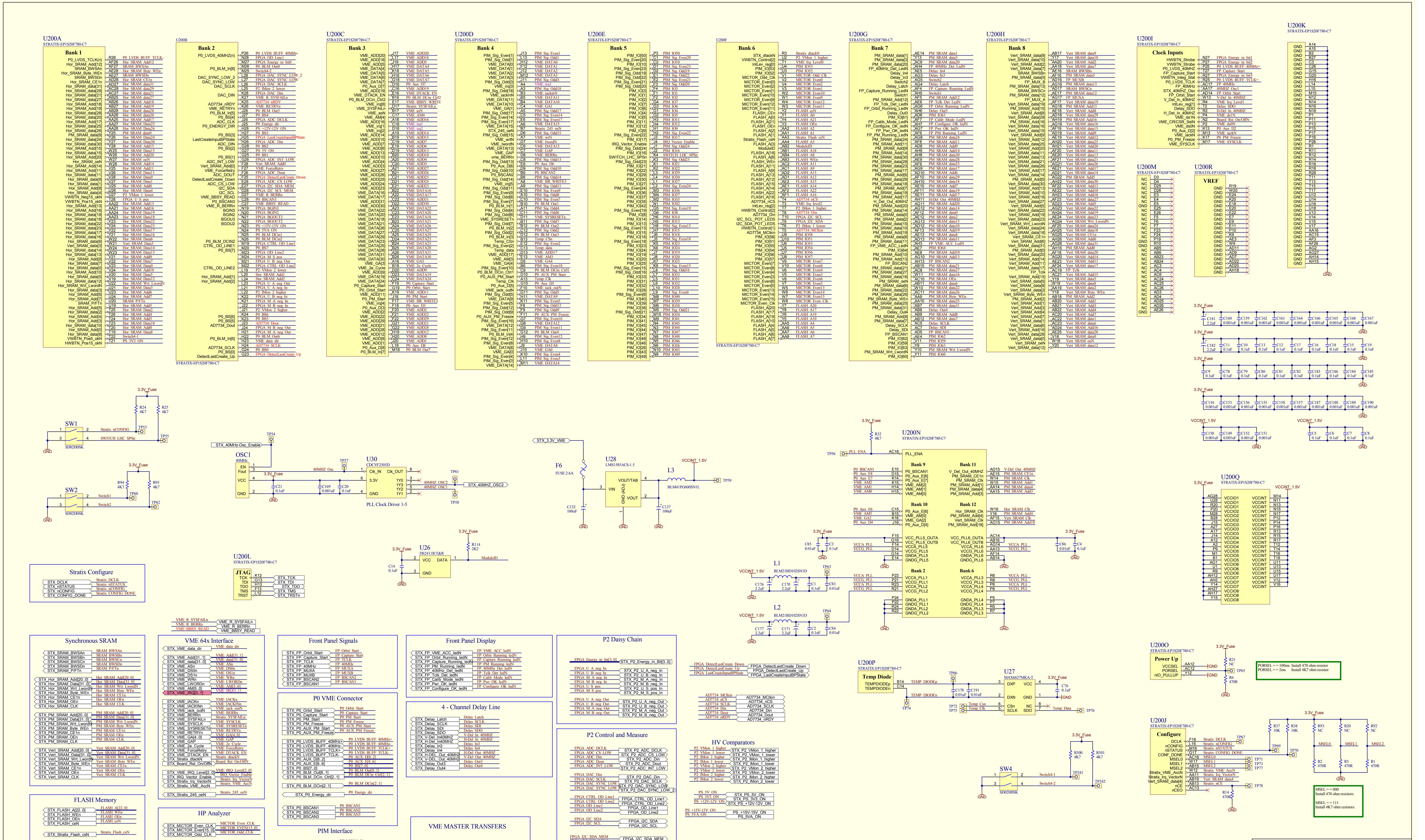
Flash Memory

CNFG_Flash_A[22..0]	Flash_A[22..0]
CNFG_Flash_weN	Flash_weN
CNFG_Flash_ceN	Flash_ceN
CNFG_Flash_oeN	Flash_oeN
CNFG_FLASH_RESETn	FLASH_RESETn

BLECS: Stratix Configuration Controller

Revision 3	CERN EDMS: EDA-01660		*CERN* based on DAB64x by TRIUMF
	Sheet #: 8 of 12	Size: B	
	Drawn by: J. Emery	Date: 05/12/2007	

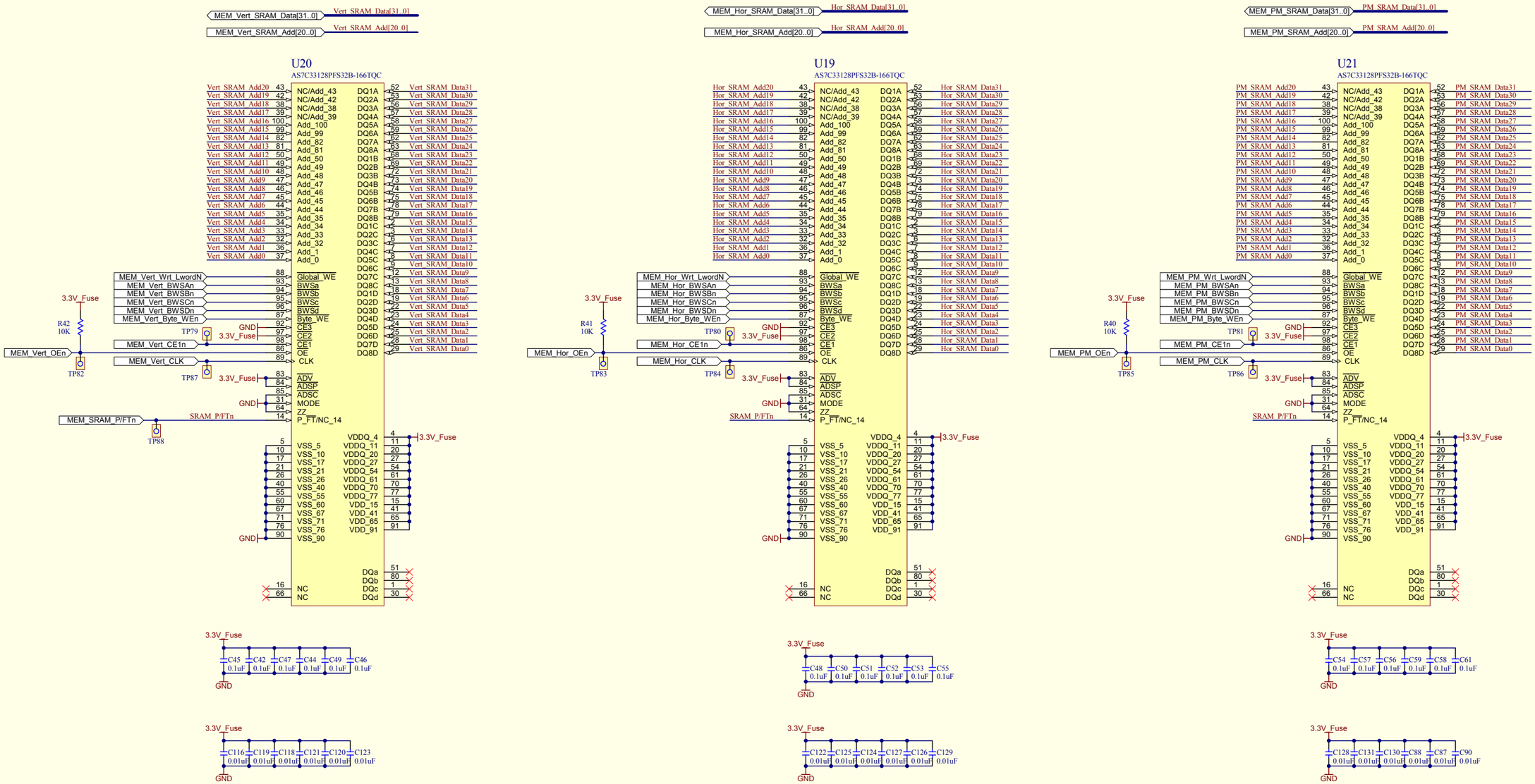
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combine



BLECS: STRATIX Controller

Revision 3	CERN EDMS: EDA-01660		CERN 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	Cannot open file G:\AHW\CERN\DAB64x\Protel-D
	Sheet #: 9 of 12	Size: D		
	Drawn by: J. Emery	Date: 05/12/2007		

File: C:\LOCAL DESIGN\altium\BLECS Combiner Altium\BLECS-Altium-Schematics\BLE2985 Combiner_Stra



BLECS: H,V & PM Synchronous SRAM

Revision 3	CERN EDMS: EDA-01660		CERN based on DAB64x by TRIUMF
	Sheet #: 10 of 12	Size: C	
	Drawn by: J. Emery	Date: 05/12/2007	
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combiner_Synch_SRAM			

Text

P1E
Z1 VME_TRSTn
Z2 GND
Z3 VME_TCK
Z4 GND
Z5 VME_TDO
Z6 GND
Z7 VME_TDI
Z8 GND
Z9 VME_TMS
Z10 GND
Z11
Z12 GND
Z13
Z14 GND
Z15
Z16 GND
Z17
Z18 GND
Z19
Z20 GND
Z21
Z22 GND
Z23
Z24 GND
Z25
Z26 GND
Z27
Z28 GND
Z29
Z30 GND
Z31
Z32 GND
IDC160

P1A
A1 P1_D00
A2 P1_D01
A3 P1_D02
A4 P1_D03
A5 P1_D04
A6 P1_D05
A7 P1_D06
A8 P1_D07
A9 GND
A10 P1_SYSCLK
A11 GND
A12 P1_DS1n
A13 P1_DS0n
A14 P1_wrN
A15 GND
A16 P1_DTACKn
A17 GND
A18 P1_ASn
A19 GND
A20 P1_IACKn
A21 P1_IACKINn
A22 P1_IACKOUTn
A23 P1_AM4
A24 P1_A07
A25 P1_A06
A26 P1_A05
A27 P1_A04
A28 P1_A03
A29 P1_A02
A30 P1_A01
A31 VME_neg12V
A32 VME_5V
IDC160

P1B
B1 P1_BBSY
B2 P1_BCLR
B3 P1_ACFAILn
B4 P1_BG0IN
B5 P1_BG0OUT
B6 P1_BG1IN
B7 P1_BG1OUT
B8 P1_BG2IN
B9 P1_BG2OUT
B10 P1_BG3IN
B11 P1_BG3OUT
B12 P1_BR0
B13 P1_BR1
B14 P1_BR2
B15 P1_BR3
B16 P1_AM0
B17 P1_AM1
B18 P1_AM2
B19 P1_AM3
B20 GND
B21 P1_SERCLK
B22 P1_SERDAT
B23 GND
B24 P1_IRQ7n
B25 P1_IRQ6n
B26 P1_IRQ5n
B27 P1_IRQ4n
B28 P1_IRQ3n
B29 P1_IRQ2n
B30 P1_IRQ1n
B31
B32 VME_5V
IDC160

P1C
C1 P1_D08
C2 P1_D09
C3 P1_D10
C4 P1_D11
C5 P1_D12
C6 P1_D13
C7 P1_D14
C8 P1_D15
C9 GND
C10 P1_SYSFAILn
C11 P1_BERRn
C12 P1_SYSRESETn
C13 P1_LWORDn
C14 P1_AM5
C15 P1_A23
C16 P1_A22
C17 P1_A21
C18 P1_A20
C19 P1_A19
C20 P1_A18
C21 P1_A17
C22 P1_A16
C23 P1_A15
C24 P1_A14
C25 P1_A13
C26 P1_A12
C27 P1_A11
C28 P1_A10
C29 P1_A09
C30 P1_A08
C31 VME_pos12V
C32 VME_5V
IDC160

P1D
D1 VME_VPC_P1
D2 GND
D3
D4
D5
D6
D7
D8
D9 P1_GAPn
D10 P1_GA0n
D11 P1_GA1n
D12 VME_3.3V
D13 P1_GA2n
D14 VME_3.3V
D15 P1_GA3n
D16 VME_3.3V
D17 P1_GA4n
D18 VME_3.3V
D19
D20 VME_3.3V
D21
D22 VME_3.3V
D23
D24 VME_3.3V
D25
D26 VME_3.3V
D27
D28 VME_3.3V
D29
D30 VME_3.3V
D31 GND
D32
IDC160

F19
Fuse 0.5A
Fuse_VPC_P1

U16
SN74ABTE16245DGGR
5V_Fuse
Fuse_VPC_P1
3.3V_Fuse
R36 10K
VME_data_dir
VME_245_oeN
VME_data8 VME_data9 VME_data10 VME_data3 VME_data4 VME_data5 VME_data6 VME_data7
VME_data0 VME_data1 VME_data2 VME_data11 VME_data12 VME_data13 VME_data14 VME_data15
1DIR 2DIR OE VCC1 VCC2 VCC3 VCC4 VCC_BIAS
1A1 1A2 1A3 1A4 1A5 1A6 1A7 1A8 2A1 2A2 2A3 2A4 2A5 2A6 2A7 2A8
1B1 1B2 1B3 1B4 1B5 1B6 1B7 1B8 2B1 2B2 2B3 2B4 2B5 2B6 2B7 2B8
P1_D08 P1_D09 P1_D10 P1_D03 P1_D04 P1_D05 P1_D06 P1_D07 P1_D00 P1_D01 P1_D02 P1_D11 P1_D12 P1_D13 P1_D14 P1_D15
VME Interface (90ma)
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8
C40 0.1uF C114 0.1uF C43 0.1uF C117 0.1uF

U14
SN74ABTE16245DGGR
5V_Fuse
Fuse_VPC_P1
TP89
R13 470R
VME_2e_cycle
CNFG_DFLT1_Lo
VME_Add16 VME_Add14 VME_Add13 VME_Add12 VME_Add11 VME_Add10 VME_Add9 VME_Add8
VME_Add15 VME_Add7 VME_Add6 VME_Add5 VME_Add4 VME_Add3 VME_Add2 VME_Add1
P1_A16 P1_A14 P1_A13 P1_A12 P1_A11 P1_A10 P1_A09 P1_A08 P1_A15 P1_A07 P1_A06 P1_A05 P1_A04 P1_A03 P1_A02 P1_A01
C38 0.1uF C112 0.1uF C41 0.1uF C115 0.1uF

U15
SN74ABTE16245DGGR
5V_Fuse
Fuse_VPC_P1
TP95 TP96
VME_2e_cycle
CNFG_DFLT2_Lo
CNFG_DFLT1_Lo
VME_LWORDn VME_Add23 VME_Add22 VME_Add21 VME_Add20 VME_Add19 VME_Add18 VME_Add17
VME_DS1n VME_DS0n VME_AM5 VME_wrN VME_AM0 VME_AM1 VME_AM2 VME_AM3
P1_LWORDn P1_A23 P1_A22 P1_A21 P1_A20 P1_A19 P1_A18 P1_A17 P1_DS1n P1_DS0n P1_AM5 P1_wrN P1_AM0 P1_AM1 P1_AM2 P1_AM3
C36 0.1uF C110 0.1uF C39 0.1uF C113 0.1uF

VME_data_dir R600 1k VME_wrN

P2_A[31..24] P2_A[31..24]
P2_D[31..16] P2_D[31..16]
P2_RETRYn P2_RETRYn

U17
SN74ABTE16245DGGR
5V_Fuse
Fuse_VPC_P2
TP91 TP92
VME_data_dir
VME_245_oeN
VME_data16 VME_data18 VME_data20 VME_data22 VME_data24 VME_data26 VME_data28 VME_data30
VME_data17 VME_data19 VME_data21 VME_data23 VME_data25 VME_data27 VME_data29 VME_data31
P2_D16 P2_D18 P2_D20 P2_D22 P2_D24 P2_D26 P2_D28 P2_D30 P2_D17 P2_D19 P2_D21 P2_D23 P2_D25 P2_D27 P2_D29 P2_D31
C32 0.1uF C106 0.1uF C35 0.1uF C109 0.1uF C179 10uF

U12
SN74ABTE16245DGGR
5V_Fuse
Fuse_VPC_P2
TP90
R12 470R
VME_ForceRetry
VME_2e_cycle
CNFG_DFLT1_Lo
VME_RETRYn
VME_Add24 VME_Add25 VME_Add26 VME_Add27 VME_Add28 VME_Add29 VME_Add30 VME_Add31
P2_RETRYn P2_A24 P2_A25 P2_A26 P2_A27 P2_A28 P2_A29 P2_A30 P2_A31
C30 0.1uF C104 0.1uF C33 0.1uF C107 0.1uF

3.3V_Fuse
R125 4K7
U18
SN74ABTE16246DGGR
5V_Fuse
Fuse_VPC_P1
3.3V_Fuse
R124 4K7
TP99
CNFG_DFLT3_Hi
CNFG_DFLT1_Lo
VME_DTACK_EN
CNFG_DFLT2_Lo
TP93 TP94
VME_DTACKn VME_ASn VME_AM4 VME_SYSFAILn VME_BERRn VME_BBSY_WRITE VME_BR_WRITE3 VME_BR_WRITE2 VME_IRQ3 VME_IRQ2 VME_IRQ1
VME_R_SYSFAILn VME_R_BERRn VME_BBSY_READ
P1_DTACKn P1_ASn P1_AM4 P1_SYSFAILn P1_BERRn P1_BBSY P1_BR3 P1_BR2 P1_IRQ3n P1_IRQ2n P1_IRQ1n
R126 470R
C34 0.1uF C108 0.1uF C37 0.1uF C111 0.1uF

P1F
MH1 MH2 mounting hole 1 mounting hole 2
IDC160
P2F
MH1 MH2 mounting hole 1 mounting hole 2
IDC160

P1_BG2IN P1_BG2IN
P1_BG3IN P1_BG3IN
P1_BG2OUT P1_BG2OUT
P1_BG3OUT P1_BG3OUT

VME_BR_WRITE[3..2] VME_BR_WRITE[3..2]
VME_BBSY_WRITE VME_BBSY_WRITE

Fuse_VPC_P2 Fuse_VPC_P2
VME_data_dir VME_data_dir

VME_Add[31..1] VME_Add[31..1]
VME_Data[31..0] VME_Data[31..0]
VME_ASn VME_ASn
VME_DTACKn VME_DTACKn
VME_LWORDn VME_LWORDn
VME_DS1n VME_DS1n
VME_DS0n VME_DS0n
VME_wrN VME_wrN
VME_AM[5..0] VME_AM[5..0]
VME_IRQ[3..1] VME_IRQ[3..1]
VME_SYSCLK VME_SYSCLK
VME_SYSRESETn VME_SYSRESETn
VME_IACKn VME_IACKn
VME_IACKINn VME_IACKINn
VME_iack_outN VME_iack_outN
VME_SYSFAILn VME_SYSFAILn
VME_BERRn VME_BERRn

VME_GA[4..0] VME_GA[4..0]
VME_GAP VME_GAP
VME_RETRYn VME_RETRYn
VME_TRSTn VME_TRSTn
VME_TCK VME_TCK
VME_TDO VME_TDO
VME_TDI VME_TDI
VME_TMS VME_TMS
VME_ForceRetry VME_ForceRetry
VME_2e_cycle VME_2e_cycle
VME_DTACK_EN VME_DTACK_EN
VME_245_oeN VME_245_oeN
CNFG_DFLT3_Hi CNFG_DFLT3_Hi
CNFG_DFLT2_Lo CNFG_DFLT2_Lo
CNFG_DFLT1_Lo CNFG_DFLT1_Lo
VME_pos12V VME_pos12V
VME_neg12V VME_neg12V

VME_R_SYSFAILn VME_R_SYSFAILn
VME_R_BERRn VME_R_BERRn
VME_BBSY_READ VME_BBSY_READ

U13
SN74ABTE16245DGGR
5V_Fuse
Fuse_VPC_P1
Direction A to B
R27 4K7 R29 4K7 R31 4K7 R30 4K7 R28 4K7 R26 4K7
VME_GAP VME_GA0 VME_SYSRESETn VME_GA2 VME_GA4 VME_IACKINn VME_SYSCLK VME_GA1 VME_GA3 VME_IACKn P1_IACKOUTn
P1_GAPn P1_GA0n P1_SYSRESETn P1_GA2n P1_GA4n P1_IACKINn P1_SYSCLK P1_GA1n P1_GA3n P1_IACKn VME_iack_outN
C28 0.1uF C102 0.1uF C31 0.1uF C105 0.1uF

VME_3.3V VME_3.3V
VME_5V VME_5V
F7 FUSE 2.6A
F5 Fuse 1.1A
TP97 TP98
3.3V_Fuse 5V_Fuse
C135 100uF C133 100uF R35 3K3 C134 100uF C136 100uF R22 4K7
LED1 HSMH-C190 LED2 HSMH-C190

BLECS: VME Interface P1/P2 Connectors

Revision 3	CERN EDMS: EDA-01660	*CERN* based on DAB64x by TRIUMF	Cannot open file TRIUMF.B MP
	Sheet #: 11 of 12	Size: C	
	Drawn by: J. Emery	Date: 05/12/2007	
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combiner_VME_Interface.SchDoc			

P0A

A1	BLMout1
A2	BLMout2
A3	BLMout3
A4	BLMout4
A5	BLMout5
A6	BLMout6
A7	BLMout7
A8	BLMout8
A9	
A10	
A11	
A12	
A13	
A14	
A15	
A16	
A17	
A18	
A19	

1725 095 2102
Harting

P0B

B1	P0_Neg5.2Vret
B2	
B3	
B4	P0_Neg5.2V
B5	
B6	
B7	P0_Neg2Vret
B8	
B9	P0_Neg2V
B10	
B11	
B12	P0_Pos5V
B13	
B14	AGND
B15	
B16	P0_Pos15V
B17	AGND
B18	AGND
B19	P0_Neg15V

1725 095 2102
Harting

P0C

C1	P0_Neg5.2Vret	P0_Neg5.2Vret
C2		
C3		
C4	P0_Neg5.2V	P0_Neg5.2V
C5		
C6		
C7	P0_Neg2Vret	P0_Neg2Vret
C8		
C9	P0_Neg2V	P0_Neg2V
C10		
C11		
C12	P0_Pos5V	P0_Pos5V
C13		
C14	AGND	AGND
C15		
C16	P0_Pos15V	P0_Pos15V
C17	AGND	
C18	AGND	
C19	P0_Neg15V	P0_Neg15V

1725 095 2102
Harting

P0D

	P0_Pos5Vret	
	P0_Pos15Vret	
	P0_Neg15Vret	
D1	Capture_Start	
D2	Auxilliary_D2	
D3	Auxilliary_D3	
D4	Auxilliary_D4	
D5	Auxilliary_D5	
D6	Auxilliary_D6	
D7	Auxilliary_D7	
D8	Auxilliary_D8	
D9	BLM_DCin1	
D10	BLM_DCin2	
D11		
D12	BS0	
D13	BS1	
D14	BS2	
D15	BS3	
D16	BS4	
D17	BS5	
D18	BS6	
D19	BS7	

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P0E

E1	Post_Mortem_Start
E2	Post_Mortem_Freeze
E3	Auxilliary_PM_Start
E4	Auxilliary_PM_Freeze
E5	Orbit_Start
E6	Auxilliary_E6
E7	Auxilliary_E7
E8	Auxilliary_E8
E9	BLM_DCout1
E10	BLM_DCout2
E11	
E12	LVDS_TCLK+
E13	LVDS_TCLK-
E14	
E15	
E16	LVDS_40MHz+
E17	LVDS_40MHz-
E18	
E19	

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P0F

GND	F1
GND	F3
GND	F5
GND	F7
GND	F9
GND	F11
GND	F13
GND	F15
GND	F17
GND	F19

GND

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Harting

U9

SN65LVDS104PW

3.3V_Fuse, GND → Vcc, Gnd
P0_BSCAN3 → EN1, EN2, EN3, EN4
LVDS_40MHz+ → R9 470R → R1
LVDS_40MHz- → R7 470R → R1
T1 → P0_LVDS_Buff_40MHz+
T2 → P0_LVDS_Buff_40MHz-

3.3V_Fuse
C26 0.1uF, C103 0.01uF
GND

U10

SN65LVDS104PW

TP100
P0_BSCAN3 → R127 470R → GND
3.3V_Fuse, GND → Vcc, Gnd
P0_BSCAN3 → EN1, EN2, EN3, EN4
LVDS_TCLK+ → R8 470R → R1
LVDS_TCLK- → R10 470R → R1
T1 → P0_LVDS_Buff_TCLK+
T2 → P0_LVDS_Buff_TCLK-

3.3V_Fuse
C27 0.1uF, C100 0.01uF
GND

U5

74LVT245DB

P0_BSCAN2 → DIR
P0_BSCAN1 → OE
AtoB=1 BtoA=0
3.3V_Fuse → 3.3V
BS7 → B1 → P0_BS7
BS6 → B2 → P0_BS6
BS5 → B3 → P0_BS5
BS4 → B4 → P0_BS4
BS3 → B5 → P0_BS3
BS2 → B6 → P0_BS2
BS1 → B7 → P0_BS1
BS0 → B8 → P0_BS0
GND

3.3V_Fuse
C22 0.1uF, C97 0.01uF
GND

U8

74LVT245DB

P0_BSCAN2 → DIR
P0_BSCAN1 → OE
AtoB=1 BtoA=0
3.3V_Fuse → 3.3V
Auxilliary_D8 → B1 → P0_Aux_D8
Auxilliary_E8 → B2 → P0_Aux_E8
Auxilliary_D7 → B3 → P0_Aux_D7
Auxilliary_E7 → B4 → P0_Aux_E7
Auxilliary_D6 → B5 → P0_Aux_D6
Auxilliary_E6 → B6 → P0_Aux_E6
Auxilliary_D5 → B7 → P0_Aux_D5
Orbit_Start → B8 → P0_Orbit_Start
GND

3.3V_Fuse
C23 0.1uF, C99 0.01uF
GND

P0_BS[7..0]
P0_Aux_D[8..2]
P0_Aux_E[8..6]
P0_BLM_Out[8..1]

P0_ENERGY_DIR → P0_ENERGY_DIR
R300 10k
GND

U11

SN74LV123ADBR

R115 10K, 3.3V_Fuse, C163 100pF
BLM_DCin1 → CLR
GND → A
P0_BLM_DCin_Ctrl1 → B
R117 10K, 3.3V_Fuse, C174 100pF
BLM_DCin2 → CLR
GND → A
P0_BLM_DCin_Ctrl2 → B
Rext/Cext, Cext, VCC, Q, Q̄
BLM_DCout1, BLM_DCout2
3.3V_Fuse → VCC
C29 0.1uF, GND
R116 10K, R118 10K, GND

U1

74LVT245DB

GND → DIR
GND → OE
AtoB=1 BtoA=0
3.3V_Fuse → 3.3V
BLMout8 → B1 → P0_BLM_Out8
BLMout7 → B2 → P0_BLM_Out7
BLMout6 → B3 → P0_BLM_Out6
BLMout5 → B4 → P0_BLM_Out5
BLMout4 → B5 → P0_BLM_Out4
BLMout3 → B6 → P0_BLM_Out3
BLMout2 R701 33R → B7 → P0_BLM_Out2
BLMout1 R700 33R → B8 → P0_BLM_Out1
GND

3.3V_Fuse
C25 0.1uF, C101 0.01uF
GND

U7

74LVT245DB

TP101
TP102
P0_BSCAN2 → DIR
P0_BSCAN1 → OE
R16 470R, GND
AtoB=1 BtoA=0
3.3V_Fuse → 3.3V
Auxilliary_D4 → B1 → P0_Aux_D4
Auxilliary_PM_Freeze → B2 → P0_Aux_PM_Freeze
Auxilliary_D3 → B3 → P0_Aux_D3
Auxilliary_PM_Start → B4 → P0_Aux_PM_Start
Auxilliary_D2 → B5 → P0_Aux_D2
Post_Mortem_Freeze → B6 → P0_PM_Freeze
Capture_Start → B7 → P0_Capture_Start
Post_Mortem_Start → B8 → P0_PM_Start
GND

3.3V_Fuse
C24 0.1uF, C98 0.01uF
GND

P0_BLM_DCin[2..1] → P0_BLM_DCin[2..1]

U70

74LVT245DB

GND → DIR
GND → OE
AtoB=1 BtoA=0
3.3V_Fuse → 3.3V
P1_BG3IN → B1 → FPGA_BGIN3
P1_BG2IN → B2 → FPGA_BGIN2
FPGA_BGOUT2 → B3 → P1_BG2OUT
FPGA_BGOUT3 → B4 → P1_BG3OUT
BLM_DCin1 → B5 → P0_BLM_DCin1
BLM_DCin2 → B6 → P0_BLM_DCin2
B7, B8
GND

3.3V_Fuse
C250 0.1uF, C251 0.01uF
GND

P1_BG2IN ↔ P1_BG2IN
P1_BG3IN ↔ P1_BG3IN
P1_BG2OUT ↔ P1_BG2OUT
P1_BG3OUT ↔ P1_BG3OUT
FPGA_BGIN[3..2] ↔ FPGA_BGIN[3..2]
FPGA_BGOUT[3..2] ↔ FPGA_BGOUT[3..2]

P0_BLM_DCin_Ctrl[2..1] → P0_BLM_DCin_Ctrl[2..1]

BLECS: VME P0 Interface

Revision 3	CERN EDMS: EDA-01660	*CERN* based on DAB64x by TRIUMF	Cannot open file TRIUMF.BMP
	Sheet #: 12 of 12	Size: B	
	Drawn by: J. Emery	Date: 05/12/2007	
File: C:\LOCAL_DESIGN\altium\BLECS_Combiner_Altium\BLECS-Altium-Schematics\BLECS_Combine			