Gesellschaft für Schwerionenforschung m.b.H.
QFW II
Preliminary Datasheet

1 General description

The QFW II ASIC, developed by the EE department of the Gesellschaft für Schwerionenforschung in Darmstadt is a highly integrated CMOS chip for measuring charge flow with a high dynamic range without range switching. The chip has a die size of 4.66 mm · 3.19 mm and is produced in an 0.35 μm CMOS technology of Austria Microsystems AG (AMS).
Features:

- 3.3 V and 5 V supply
- four converter channels
- internal references, no external components for converters
- positive and negative currents from 300 fA to 180 μA
- current overflow detection
- integrated pulse counting and data readout system
- total power dissipation 630 mW

1.1 Pinout and Pinnames

The chip is housed in a 64-pin CQFP package as shown in figure 1. The pinout can be found in table 1.

GNDD, GNDA Ground connection for the digital and analog parts.

VDDD, VDDA 3.3 V power supply for the digital and analog parts.

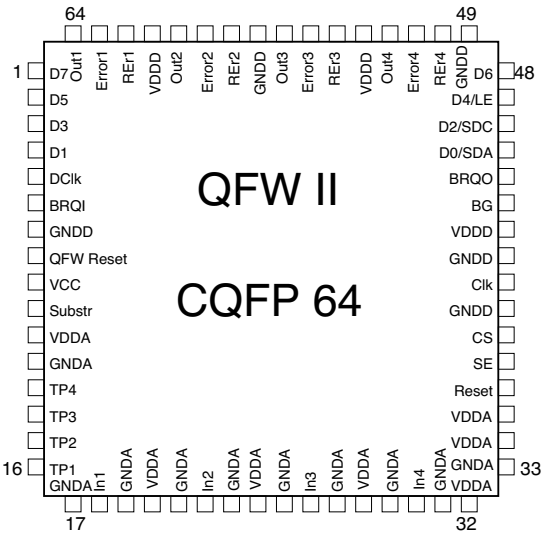

Figure 1: packaging diagram of the QFW II ASIC

VCC 5 V power supply for the analog part.

In n Current input of the nth converter channel. To aim a minimum of leakage current no ESD protection diodes are connected to the inputs In1 to In3. In4 is protected by standard ESD protection diodes.

Out n Frequency output of the nth converter channel.

Error n Output of the Errorregister of the nth converter channel. The Error output is activ high.

Reset Error n Reset input to clear the Errorregister of the nth converter channel. Reset Error is

Pin	Direction	Name
1	in/out	D7
2	in/out	D5
3	in/out	D3
4	in/out	D1
5	in/out	$\overline{\text{DClk}}$
6	in	BRQI
7	pwr	GNDD
8	in	$\overline{\text{QFWReset}}$
9	pwr	VCC
10	pwr	Substrate
11	pwr	VDDA
12	pwr	GNDA
13	out	TP4
14	out	TP3
15	out	TP2
16	out	TP1
17	pwr	GNDA
18	in	In 1
19	pwr	GNDA
20	pwr	VDDA
21	pwr	GNDA
22	in	In 2
23	pwr	GNDA
24	pwr	VDDA
25	pwr	GNDA
26	in	In 3
27	pwr	GNDA
28	pwr	VDDA
29	pwr	GNDA
30	in	In 4
31	pwr	GNDA
32	pwr	VDDA

Pin	Direction	Name
33	pwr	GNDA
34	pwr	VDDA
35	pwr	VDDA
36	in	$\overline{\text{Reset}}$
37	in	$\overline{SE}$
38	in	$\overline{CS}$
39	pwr	GNDD
40	in	Clk
41	pwr	GNDD
42	pwr	VDDD
43	in	BG
44	in	BRQO
45	in/out	D0 / SDC
46	in/out	D2 / SDA
47	in/out	D4 / LE
48	in/out	D6
49	pwr	GNDD
50	in	Reset Error 4
51	out	Error 4
52	out	Out 4
53	pwr	VDDD
54	in	Reset Error 3
55	out	Error 3
56	out	Out 3
57	pwr	GNDD
58	in	Reset Error 2
59	out	Error 2
60	out	Out 2
61	pwr	VDDD
62	in	Reset Error 1
63	out	Error 1
64	out	Out 1

Table 1: Pinout

active high and has an internal pull-down resisitor.

QFW Reset Reset input to clear the charge to frequency converter. QFW Reset is active low and has an internal pull-up resistor.

TP1 ... TP4 Four testsignals of the first charge to frequency converter channel.

BRQI Busrequest daisy chain input of the bus arbitration unit. BRQI is active high and has an internal pull down resistor.

BRQO Busrequest daisy chain output of the bus arbitration unit. BRQO is active high.

BG Bus grant input of the bus arbitration unit. BG is active high and has an internal pull-down resistor.

D0 ... D7 Databus for configuration and readout. In serial configuration mode, some pins have special functions. In this case, D0 is used as a serial data in (SDA) pin. D2 is used as serial clock and D4 is used as data latch enable. The data lines are active high.

DClk Clock for data transfer. The dataclock signal is low active.

Clk 10 MHz System Clock input. Only required in the data acquisition mode.

CS Chip select for the configuration data transfer. The chip select input is low active and has an internal pull-up-resistor.

SE Serial enable sets the configuration data transfer into the serial mode. The SE input is low active and has an internal pull-up resistor.

Reset initializes the whole chip. The configuration registers are set to initial state. The reset input is low active and has an internal pull-up resistor.

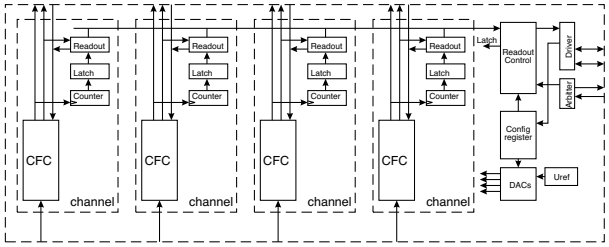

Figure 2: blockdiagram of the QFW II ASIC

1.2 Block diagram

In figure 2 a blockdiagram of the QFW ASIC is shown. The chip has four independend charge to frequency converter channels. The output of each converter is counted in 16 bit counters which are latched periodicaly. A channel readout unit sends the counting data to the readout control unit.

For communication with external readout components an 8-bit databus is used. After occupying the databus by the bus arbiter, the readout controller sends the counting data in well defined readout data frames to this bus. The same bus is used to send configuration data to the QFW-chip. These data are latched in the configuration register.

For operation the charge to frequency converter needs four different reference voltages. To adjust these voltages for best converter performance, four 10-bit digital to analog converters are implemented, using a common bandgap voltage reference.

2 Functional description

2.1 charge to frequency converter

Figure 3 shows a principle diagram of the charge to frequency converter core which is implemented twice for each converter channel. After initialization the first converter core is connected to the charge input. The incoming charge is integrated on the capacitor C_i. The output voltage of the integrator is continously compared with a threshold voltage which is generated by an 4 bit digital to analog converter (DAC) getting the input data from a 4 bit counter. Each time the integrator output exceeds the threshold voltage the counter is incremented,

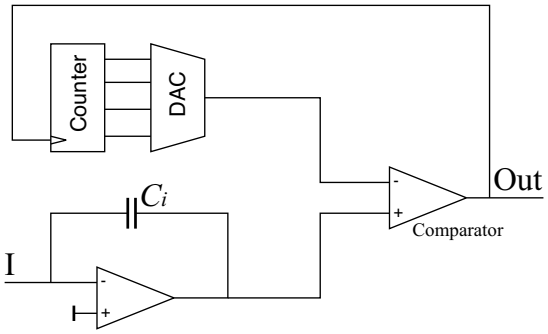

Figure 3: principle schematics of the charge to frequency converter core

so the threshold voltage is increased by one voltage step. When the counter reaches the maximum value the second converter core takes over the operation and the first one is cleared.

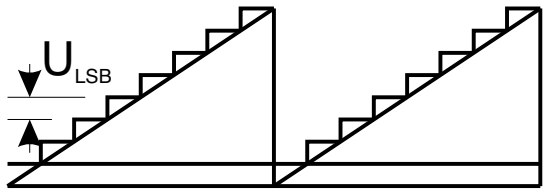

Figure 4: principle transiants of the two ramps

The charge, which is needed for each pulse is given by the step voltage of the DAC U_{LSB} and the integration capacitance C_i by $Q = U_{LSB} \cdot C_i$. The output frequency f increases linear with the input current I: $f = I/Q$.

2.2 Voltage References

For operation the charge to frequency converter needs four reference voltages, $\mathrm{V_{zero}}$, $\mathrm{V_{low}}$, $\mathrm{V_{high}}$ and $\mathrm{V_{full}}$. During initialization, the integrator is cleared to $\mathrm{V_{zero}}$, so charge integration starts from this point. The output voltage range of the DAC is given by $\mathrm{V_{low}}$ and $\mathrm{V_{high}}$. The output voltage is

$$U_{Out} = \mathrm{V_{low}} + \mathrm{D_{Counter}} \cdot (\mathrm{V_{high}} - \mathrm{V_{low}})/16$$

so the lowest output Voltage is $\mathrm{V_{low}}$ and the Step voltage

$$U_{LSB} = \frac{\mathrm{V_{high}} - \mathrm{V_{low}}}{16}.$$

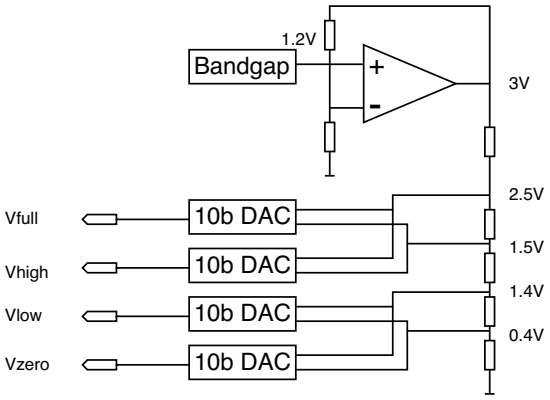

Figure 5: blockdiagram of the reference voltage generation

The highest possible threshold level is $\mathrm{V_{low}} + 15 \cdot U_{LSB}$ which is one U_{LSB} below $\mathrm{V_{high}}$

$\mathrm{V_{full}}$ has to be greater than $\mathrm{V_{high}}$. In normal operation the integrater ouput voltage will never exceed $\mathrm{V_{full}}$. If this happens nevertheless, it is an indication for an converter error i.e. a current overflow.

For reference voltage generation four voltages (0.4 V, 1.4 V, 1.5 V and 2.5 V) are derived from an internal 1.2 V bandgap voltage reference as shown in figure 5. These voltages are used as references for four 10 bit DAC, each for one of the four needed reference voltages, so $\mathrm{V_{zero}}$ and $\mathrm{V_{low}}$ can be adjusted in the range from 0.4 V to 1.4 V and $\mathrm{V_{high}}$ and $\mathrm{V_{full}}$ can be adjusted in the range from 1.5 V to 2.5 V. The resolution of each DAC is about 1 mV.

The digital inputs of the DACs are connected to the configuration registers described in section 2.4. The output voltages can be calculated as follows:

$$\begin{aligned} \mathrm{V_{zero}} &= 0.4\ \mathrm{V} + D_{\mathrm{zero}}/1024\ \mathrm{V}^{-1} \\ \mathrm{V_{low}} &= 0.4\ \mathrm{V} + D_{\mathrm{low}}/1024\ \mathrm{V}^{-1} \\ \mathrm{V_{high}} &= 1.5\ \mathrm{V} + D_{\mathrm{high}}/1024\ \mathrm{V}^{-1} \\ \mathrm{V_{full}} &= 1.5\ \mathrm{V} + D_{\mathrm{full}}/1024\ \mathrm{V}^{-1} \end{aligned}$$

A typical operating condition for the charge to frequency converter is $\mathrm{V_{low}} = 0.65$ V and $\mathrm{V_{high}} =$

2.25 V. This leads to a step voltage U_{LSB} = 100 mV. By adjusting V_{low} and V_{high} variations of the integration capacity C_i can be compensated. Charge injection effects during clearing and switching between the integrators can be corrected by adjusting V_{zero} which has to be about one U_{LSB} below V_{low}. V_{full} should be the same as V_{high}. In positive current mode adjusting this voltage could be used to correct charge injection effects.

2.3 Eventcounter

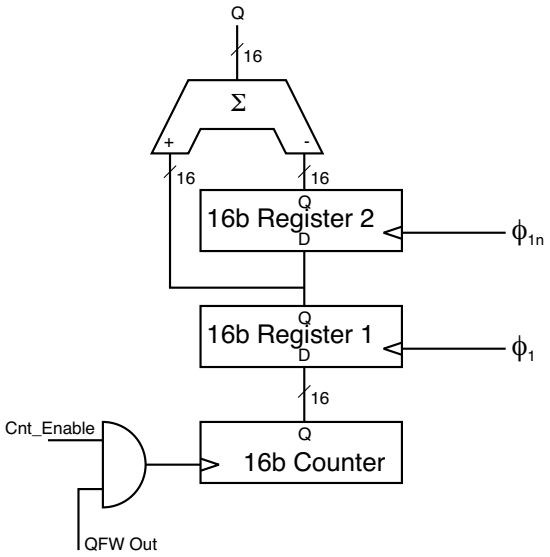

Figure 6: blockdiagram of the eventcounter

The output of each charge to frequency converter which is connected to an output pin is also used as input of an internal event counter. The block diagram of this event counter is shown in figure 6. If the common configuration signal *cnt_enable* is active, the pulses from the converter are counted in a 16 bit binary counter. To avoid deadtime, this counter is running continously. After a fixed gatetime, the countingstate is latched in register 1 by the clocksignal ϕ_1. In register 2 the countingstate of the last readout periode is latched, so the number of events during the last gatetime periode can be calculated by a subtractor as shown in figure 6. After readout the new countingstate is latched in register 2 by the clocksignal ϕ_{1n} for the next readout cycle.

2.4 Configuration Unit

For setup and configuration of the chip a set of ten 8 bit configuration registers is used. With the *reset* signal these registers are set to default values, so the chip is operational in a basic mode without any reference adjusting and internal data acquisition. If more advanced features of the chip should be used, individual setting of the configuration registers is necessary. This could be done in a parallel or a serial mode.

2.4.1 Parallel Configuration Mode

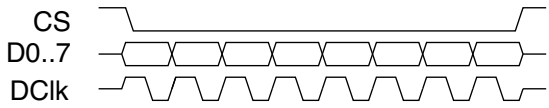

Figure 7: timing diagram of parallel configuration

Figure 7 shows a timing diagram of the QFW-chip configuration in parallel mode. In this mode the 8 bit databus is used for data transfer. To invoke the data transfer the *Chip Select* input (Pin 38) has to be set to low level. *Serial Enable* (Pin 37) has to stay at high level in parallel mode. For transfering one byte the data has to be put on the databus. When the data is stable it can be written to the configuration register with a negative edge of the *Data Clock* input (Pin 5). With the first negative edge of *data clock* after *chip select* went low, register 0 is written, each following negative edge writes data in the following registers.

2.4.2 Serial Configuration Mode

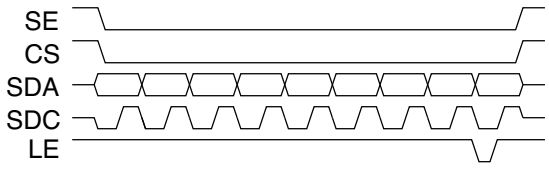

Figure 8: timing diagram of serial configuration

In some cases users may not need the internal data acquisition so the 8 bit databus is not needed during operation. In this cases it could be desirable to have a less amount of digital connections to the chip. For this reason also a serial configuration

mode was implemented. Figure 8 shows the timing of serial configuration.

To invoke the serial configuration mode *chip select* input (Pin 38) and *serial enable* input (pin 37) has to be set to low level. Serial data has to be connected to *SDA* input (pin 46). Each data bit beginning with bit 7 is shifted into the serial receiver on the positive edge of *SDC* (pin 45). When a byte is completed, it can be written into the configuration registers by the negative edge of *LE* (pin 47). As in parallel mode also in serial mode register 0 is written with the first negative edge of *LE* after *chip select* went low.

2.4.3 Configuration Register

The QFW II ASIC has ten 8 bit configuration registers, numbered from 0 to 9. During configuration data transfer register 0 is written first, register 9 is written last.

Register 0 is the main configuration register. The bits are used as following:

Bit 7: PosNeg If PosNeg is set to one, the charge to frequency converters are sensitive for positive currents. In the other case, negative currents are measured.

Bit 6: CSel With CSel the value of the integration capacity can be choosen. If this bit is set to zero, an integration capacity of 2.5 pF leading to a charge resolution of 0.25 pC is choosen. If it is set to one, the integration capacity is ten times higher. Due to the lower charge resolution of 2.5 pC per pulse, the maximum input current increases by one order of magnitude.

Bit 5: Unused

Bit 4: Cnt_Enable To enable the onchip readout counters this bit has to be set to one. If it is set to zero, the counters are disabled.

Bit 3: GC1, Bit 2: GC0 With the Gate Control bits the readout periode time is set. Four settings are possible:

GC1	GC0	Readout periode
0	0	100 μs
0	1	500 μs
1	0	800 μs
1	1	1000 μs

This timing information assumes an input clock frequency of 10 MHz.

Bit 1: ROC1, Bit 0: ROC0 With the Readout Control bits the data transfer rate during data pushing is set. Four settings are possible:

ROC1	ROC0	Data rate
0	0	10.00 MByte/s
0	1	5.00 MByte/s
1	0	2.50 MByte/s
1	1	1.25 MByte/s

This data rate information assumes an input clock frequency of 10 MHz.

After reset, all bits of register 0 are set to zero.

Register 1 is the chip-ID register. As it is possible to connect more than one QFW II ASIC in a daisy chain application it is necessary to identify the readout data frames of each chip. This is done by a chip-ID byte in each dataframe. This chip-ID byte is given by the entry of the chip-ID register. After reset the chip-ID register is set to zero.

Register 2 and 3 are the data registers of the V_{zero} reference voltage DAC. Register 2 contains bits 8 and 9, register 3 contains bits zero to seven. After reset D_{zero} is set to 150_d or 00.10010110_b.

Register 4 and 5 are the data registers of the V_{low} reference voltage DAC. Register 4 contains bits 8 and 9, register 5 contains bits zero to seven. After reset D_{low} is set to 250_d or 00.11111010_b.

Register 6 and 7 are the data registers of the V_{high} reference voltage DAC. Register 6 contains bits 8 and 9, register 7 contains bits zero to seven. After reset D_{high} is set to 750_d or 10.11101110_b.

Register 8 and 9 are the data registers of the V_{full} reference voltage DAC. Register 8 contains bits 8 and 9, register 9 contains bits zero to seven. After reset D_{full} is set to 750_d or 10.11101110_b.

2.5 Data Acquisition Unit

In the QFW II ASIC an autonomous data acquisition unit is implemented. This daq unit collects the counting data from all converter event counters, creates defined data frames and sends them to an external 8 bit data bus. To allow more than one QFW II chip to use the same data bus a bus arbitration unit is also implemented.
As a possible application a fifo memory can be controlled by the QFW II daq directly.

2.5.1 Bus Arbitration

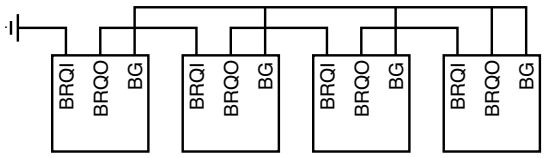

Figure 9: daisy chain connection of the bus arbitration units

The bus arbitration is done in a typical daisy chain application. The arbitration unit has a daisy chain busrequest input and busrequest output. The busrequest output of the last QFW II chip in the chain has to be connected to the bus grant inputs of each chip, as shown in figure 9.

If one of the chips wants to occupy the data bus, it has to wait, until any other chip releases the bus. When the bus is vacant, indicated by an inactive BG input, the bus arbitration unit checks, if a chip with higher priority requests the bus, indicated by an active BRQI input. If BRQI is active, the chip has to transfer this higher priority busrequest to its BRQO output and wait until the other chip has sent its data.

If BRQI is inactive, the bus arbitration unit can request the bus by setting BRQO to high level. When the BG input gets high and BRQI is still low, the data bus is occupied by this chip. As long as BG stays at high level, no other QFW II can occupy the data bus.

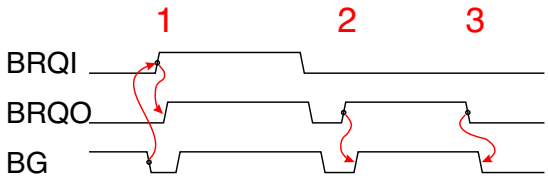

Figure 10: timing diagram of bus arbitration

Figure 10 shows a timing diagram of the bus arbitration signals. In situation 1 the bus gets vacant and a higher priority arbitration unit requests the bus. The high level on the BRQI input is passed through to the BRQO output. In situation 2 the bus gets vacant again, but no higher priority arbitration unit requests the bus. The arbitration unit can request the bus by setting BRQO to high level. In situation 3 the data is transmitted and the arbitration unit releases the bus .

2.5.2 Data pushing

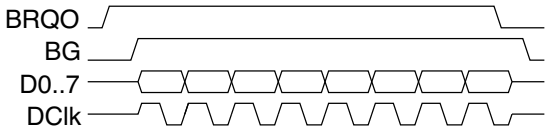

Figure 11: timing diagram of data pushing

When the databus is occupied by the bus arbitration unit, the readout data is sent to the databus in a defined dataframe format. As shown in figure 11 after bus arbitration each databyte is put on the databus. When data is stable a negative edge of the data clock output (pin 5) indicates the valid data on the databus. The datatransfer starts with byte 0. After the whole dataframe is sent, the databus is released and databus and data clock outputs go to high ohmic state.

2.5.3 Data Frame Format

Each dataframe starts with a preamble of four bytes. The first byte is the chip-ID, followed by 2 bytes containing the counterstate of a 16 bit readoutcounter. This counter is incremented after each data readout. The last byte of the preamble is a status byte which is used as following:

Bit 0: ROCSel0, Bit 1: ROCSel 1 The ROCSel bits indicate the selection of the readout speed. Four selections are possible:

ROCSel1	ROCSel0	Data rate
0	0	10.00 MByte/s
0	1	5.00 MByte/s
1	0	2.50 MByte/s
1	1	1.25 MByte/s

This data rate information assumes an input clock frequency of 10 MHz.

Bit 2: GSel0, Bit 3: GSel 1 The GSel bits indicat the status of the gate time periode selection. Four selections are possible:

GSel1	GSel0	Gate time periode
0	0	100 μs
0	1	500 μs
1	0	800 μs
1	1	1000 μs

This timing information assumes an input clock frequency of 10 MHz.

Bit 4: Readout Error If it was not possible to send readout data to the databus during one gatetime periode an readout error flag is set. this flag is send in bit 3 of the status byte of the next readout frame, to indicate that the data might by corrupted.

If there is an internal error in the main state machine, the readout error flag is also set.

Bit 5 - 7: In bits 0 to 2 the number of following channel information blocks is coded. In QFW II chip this is fixed to four channel information blocks, but in later chips it might by possible to use zero suppression.

After the preamble is sent the channel information blocks are following. Each channel information block contains three bytes. The first byte contains Bit zero to seven of the channel event counter. Bits 9 to 15 of this counter follow in the second byte. The third byte is the channel status byte. The bits of this status byte are used as following:

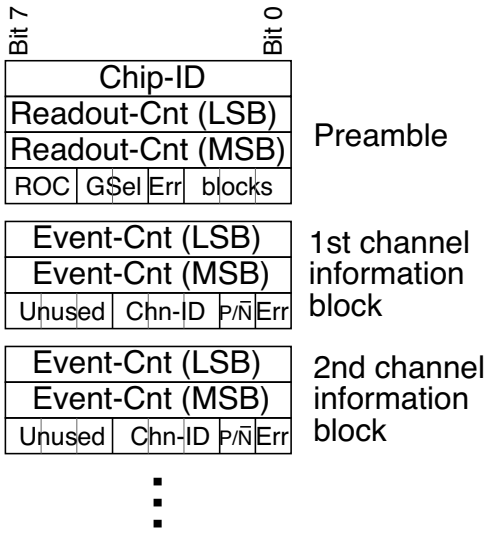

Figure 12: structure of the readout dataframe

Bit 0: Error If the maximum input current is exceeded and the comparator — counter — dac — chain can not follow the integrator ramp voltage an error register is set and bit 0 of the channel status register is one.

When the error status is transmitted, the converter is reseted and the error register is cleared automaticaly.

Bit 1: PosNeg If this bit is one, the charge to frequency converter was sensitive to positive currents, otherwise it was sensitive to negative currents.

Bit 2 - 4: Channel - ID The four converter channels in the QFW II ASIC are numbered from zero to three. These three bits are set to the channel number the channel information block belongs to.

Bit 5 - 7: unused

In figure 12 the structure of the readout dataframe is shown in a graphical way. In this figure two channel information blocks are shown after the preamble.

3 Static and Dynamic Parameter

3.1 Converter characteristics

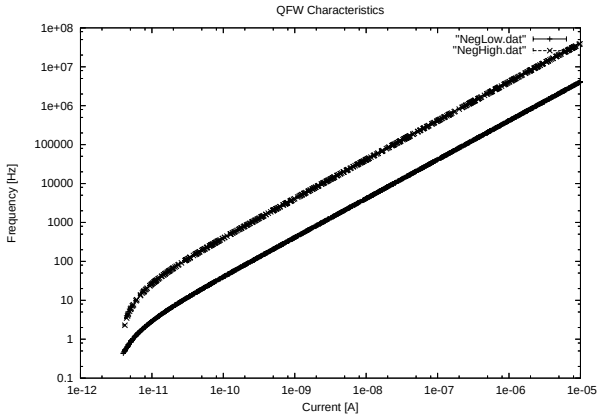

Figure 13: Converter characteristics for negative currents

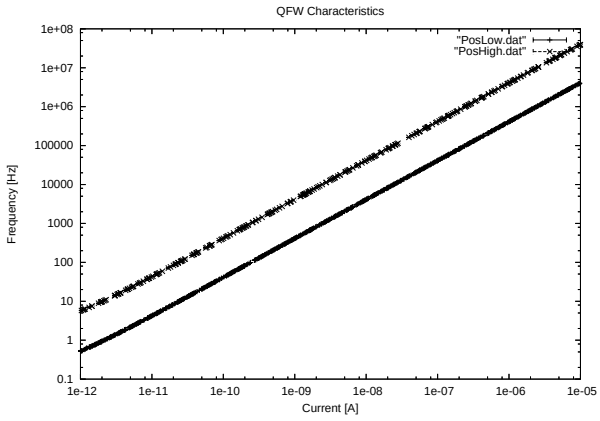

Figure 14: Converter characteristics for positive currents

Figures 13 and 14 show measured converter characteristics for negative and positive currents over seven orders of magnitude in current. In both cases the output frequency of the converter is plotted over the input current in low and high resolution mode.
To estimate the behavior at very small currents the current range up to 10 pA is plotted in figures 15 and 16. One can see that the characteristics do not cross the origin of the axis in both cases due to leakage currents. In case of negative currents a minimum input current in the order of 3 pA is needed to genarate an output signal. In case of positive currents a dark rate in the order of 1 Hz is caused by leakage currents. By substraction of this dark rate measurements of positive currents below 100 fA are possible.

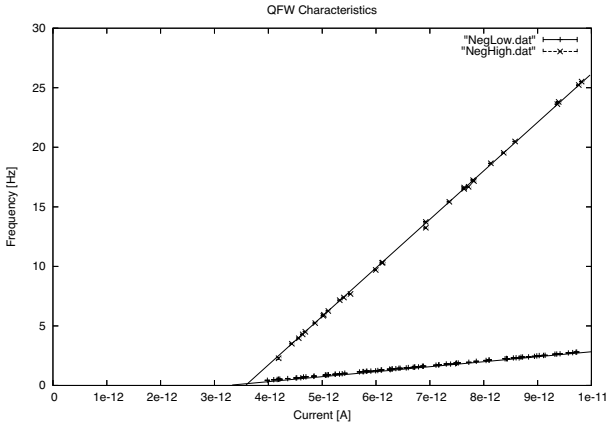

Figure 15: Converter characteristics for small negative currents

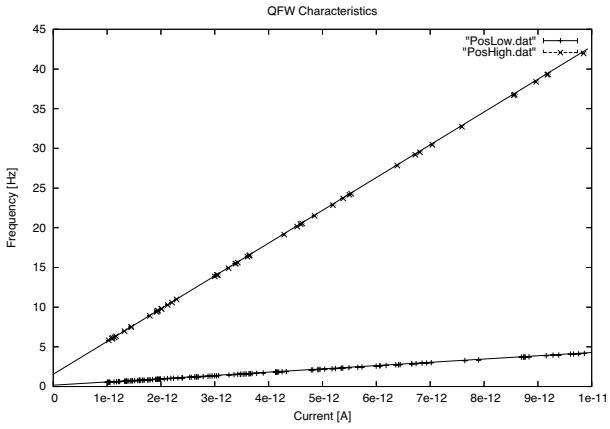

Figure 16: Converter characteristics for small positive currents

to get an information about the linearity of the

current to frequency converter in figures 17 to 20 the relative deviation of the measured frequency from linear behavior is plotted over the input current. Figures 17 and 18 show this for negative currents in low and high resolution mode. At very low currents a large statistical spread du to very low ouput frequency and limited measuring gate time are observable. Internal delays of the comparator, core decreases with increasing frequencis a charge loss due to this dead time becomes more significant at higher output frequencies. this leads into a decline of the output frequency starting at currents between 100 nA and 1 μA as it is visible in figures 17 and 18. As in high resolution mode the output frequency is ten times higher here the effect is more significant. In figure 19 and 20 the same mesure-

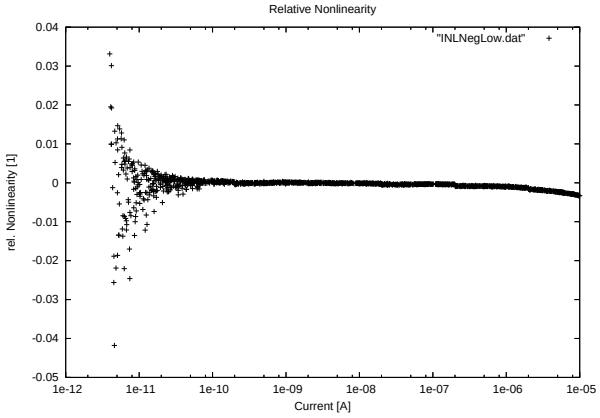

Figure 17: Relative nonlinearity for negative currents in the low resolution mode

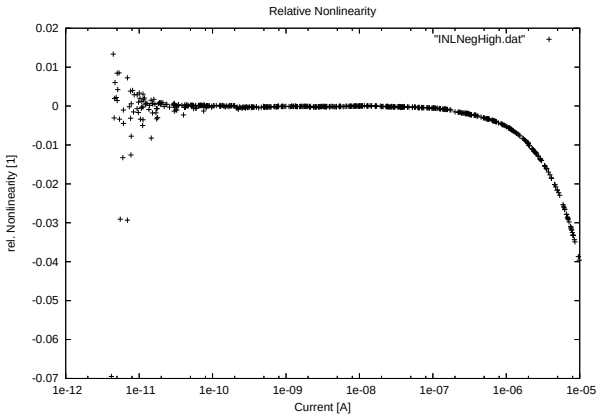

Figure 18: Relative nonlinearity for negative currents in the high resolution mode

counter and DAC in the converter cores lead into a small dead time during overtaking operation from one converter core to the other. As this dead time is constant and the measuring time of one converter

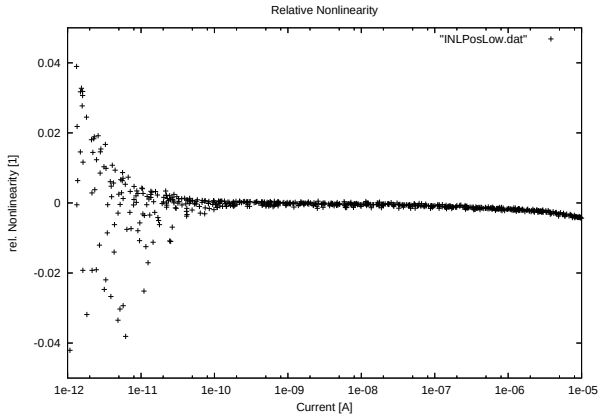

Figure 19: Relative nonlinearity for positive currents in the low resolution mode

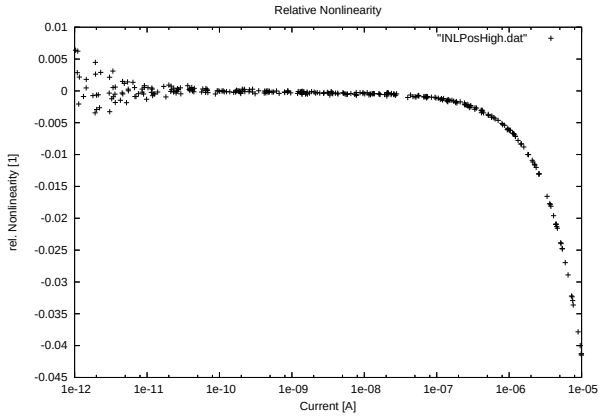

Figure 20: Relative nonlinearity for positive currents in the high resolution mode

ments are shown for positive currents. In all cases the plots show the excellent linearity of the device over a very large dynamic range.

3.2 Static Parameter

3.2.1 Power supply

Parameter	min	typ	max
VDDA		3,3 V	
VDDD		3,3 V	
VCC		5,0 V	
IDDA		150 mA	
IDDD		40 mA	
ICC		1 mA	
Total Powerdissipation		630 mW	

3.2.2 Logic Level

Parameter	min	typ	max
V_{HI}	2.8 V	3.3 V	
V_{LI}		0 V	0.5 V
V_{HO}		3.3 V	
V_{LO}		0 V	
I_{Out}		4 mA	

3.3 Dynamic Parameter

3.3.1 Level transistions

Parameter	min	typ	max
t_{OR}		960 ps	
t_{OF}		760 ps	
t_{IR}			
t_{IF}			

All output data at 25° C , VDD = 3.3 V and 10 pF load.

3.3.2 Converter characteristics

Parameter			min	typ	max
Charge resolution	C_{Int} = 2.5 pF	pC	0.237	0.241	0.245
	C_{Int} = 25 pF	pC	2.35	2.40	2.43
I_{max}	C_{Int} = 2.5 pF	μA		13	
	C_{Int} = 25 pF	μA		130	
I_{leak}	negative Currents	pA	2	3.5	5.5
	positive Currents	pA	-0.5	-0.3	-0.1
Temperature coefficient	C_{Int} = 2.5 pF				
	C_{Int} = 25 pF				
Pulse width		ns		7.4	

Current Range with integral nonlinearity better than 1 % or 0.1 %.

Current Direction	Charge Resolution	≤ 1 %		≤ 0.1 %	
		min	max	min	max
Negative	Low	20 pA	10 μA	300 pA	200 nA
	High	25 pA	2,2 μA	250 pA	2,5 nA
Positive	Low	1 pA	10 μA	20 pA	250 nA
	High	3 pA	2 μA	100 pA	50 nA

Integral nonlinearity in the current range from 50 pA to 1 μA and 50 pA to 10 μA

Current Direction	Charge Resolution	50 pA to 1 μA		50 pA to 10 μA	
		min	max	min	max
Negative	Low	-0,3 %	+0,2 %	-0,35 %	+0,2 %
	High	-0,5 %	+0,5 %	-4 %	+0,5 %
Positive	Low	-0,15 %	+0,1 %	-0,4 %	+0,07 %
	High	-0,6 %	+0,2 %	-4,5 %	+0,2 %

3.3.3 Data Readout

Parameter	min	typ	max
Readout clock frequency		10 MHz	
Duty cycle	20 %		80 %

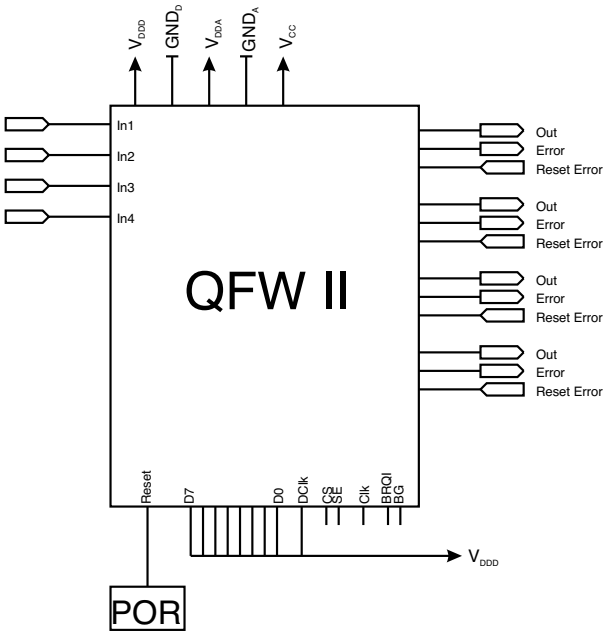

Figure 21: simpliest way of operation

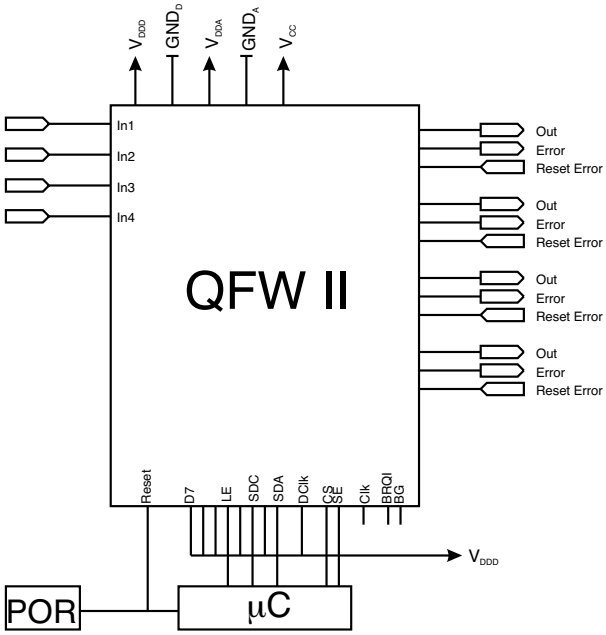

Figure 22: operation of a single QFW II with serial configuration and no readout

4 Applications

The most simple way to use the QFW II ASIC for charge flow measurements is shown in figure 21. This application ist done without any configuration, the asic is initialized by a power on reset generator. In this case the default configuration with negative currents and an integration capacitor of 2.5 pF is used. The reference voltages are also set to default values.

All input pins have internal pull-up or pull-down resistors, so no external pull-ups or pull-downs are neccessary if the input pins are not used. The tri-state databus has no internal pull-up resistors, so *D0* to *D7* and *DClk* should be connected to high level externaly.

If the maximum current is exceeded in any channel the error register of this channel will be set. This is indicated by an active error output of this channel. The converter channel will switch to an inactive state in this case, so the user has to clear this state by activating the reset error input.

All eventcounting, readout and data processing has to be done externaly.

If the internal eventcounting and data readout is not needed, but another configuration than the default configuration is needed, figure 22 shows a possible application in this case. The configuration of the chip after power on is done in serial mode by a microcontroller. The serial mode is used to save data connections between microcontroller and QFW II ASIC.

All input pins have internal pull-up or pull-down resistors, so no external pull-ups or pull-downs are neccessary if the input pins are not used. The tri-state databus has no internal pull-up resistors, so *D1*, *D3*, *D5* to *D7* and *DClk* should be connected to high level externaly.

Figure 23 shows a more sophistcated application of four QFW II ASIC. In this case the internal eventcounting and readout is used. The bus arbitration units of all chips are connected in a daisy chain and the data and data clock outputs

are connected to a common databus which is connected to the input of a fifo memory.

The configuration is done in parallel mode by a micro controller. To be able to write different configuration data to the four chips the microcontroller sends addressdata to a decoder to select a single QFW II ASIC for configuration. If this feature is not needed one can also connect all chip select inputs to a common configuration enable line. To avoid sending data to the databus by an already configured QFW II ASIC the microcontroller has to occupy the databus for configuration.

For data processing keep in mind that the configuratin data is also written to the fifo memory.

The converter frequency and error outputs are also available in this operation mode, but the user must not reset the converter error registers externaly. This is done internaly by the data acquisition unit.

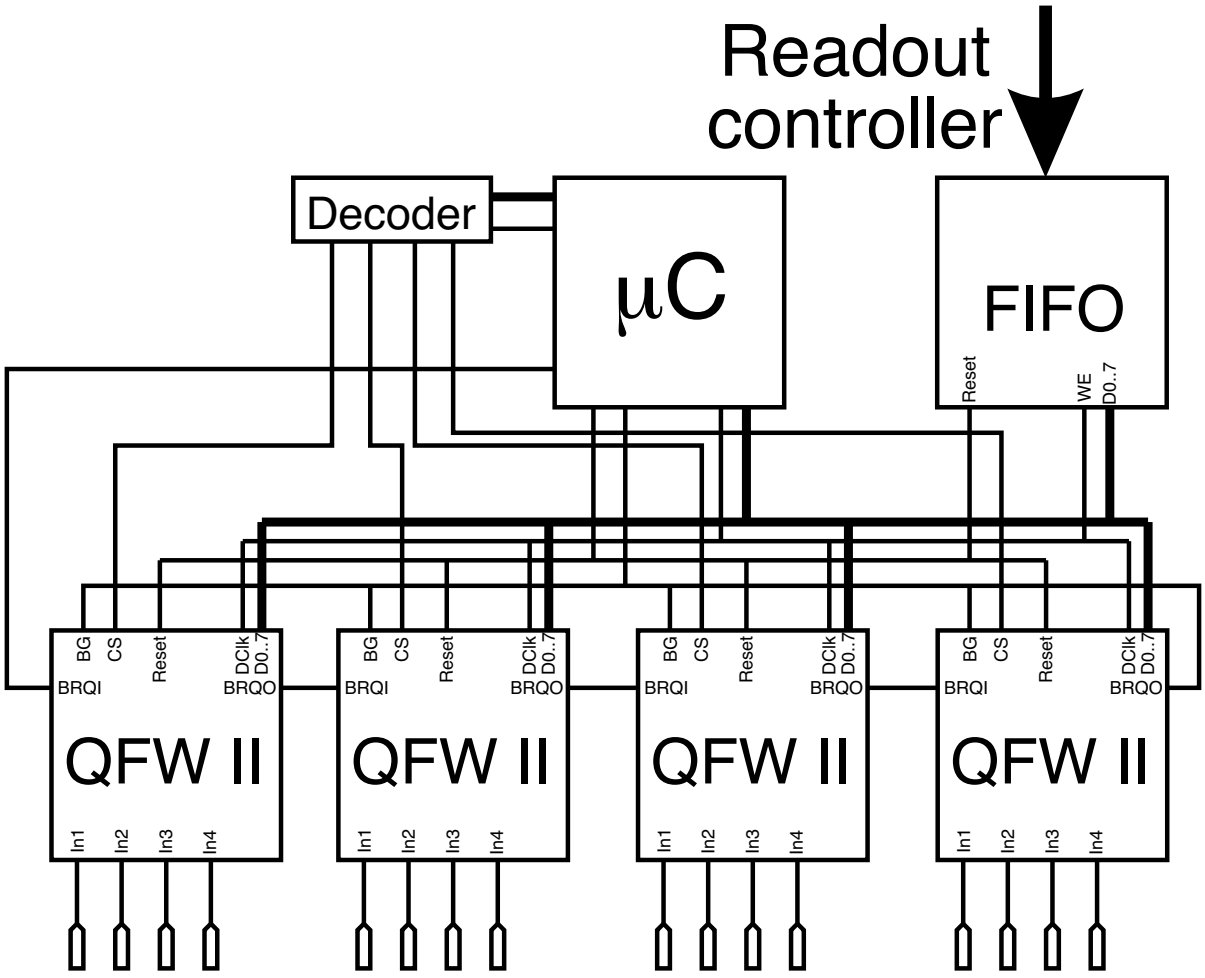

Figure 23: operation of a four QFW II asics with parallel configuration and readout through an fifo memory

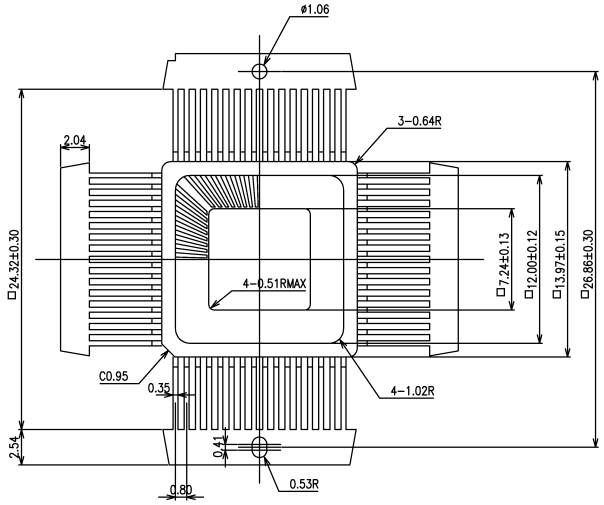

Figure 24: topview of used package. All dimensions in mm

5 Mechanical Parameter

Figures 24 and 25 show all mechanical dimensions of the used ceramic quad flat pack (CQFP64) package. All dimensions are given in mm. The leads are cutted 3.2 mm from the housing body.

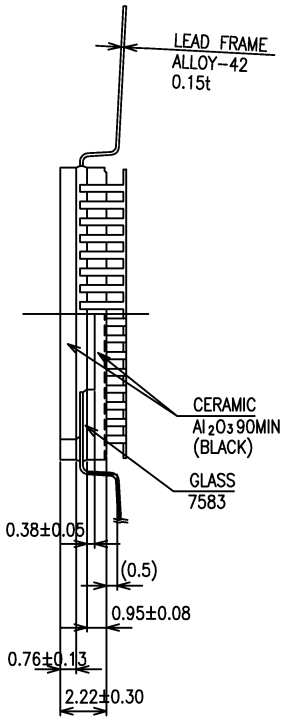

Figure 25: sideview of the used package. All dimensions in mm