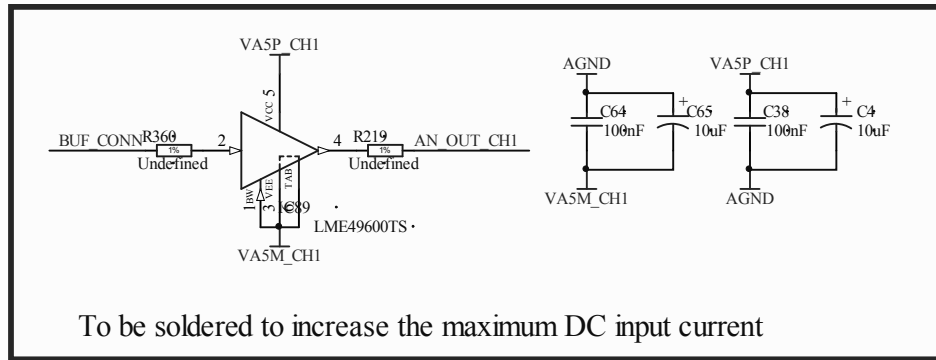
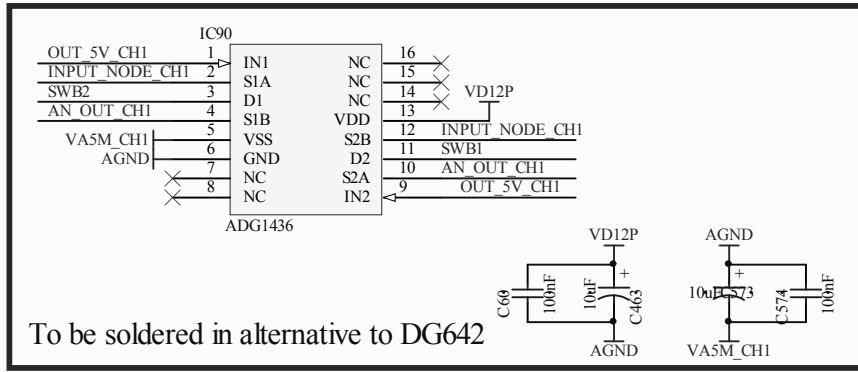
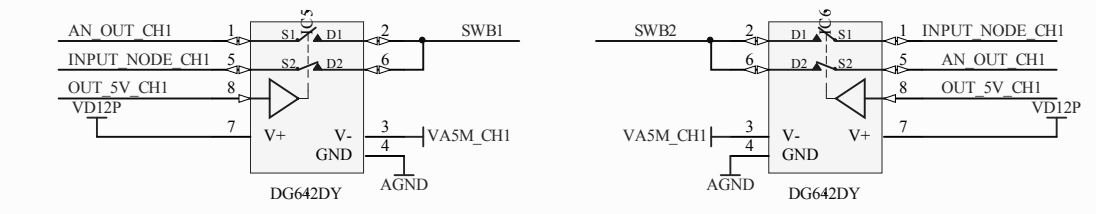


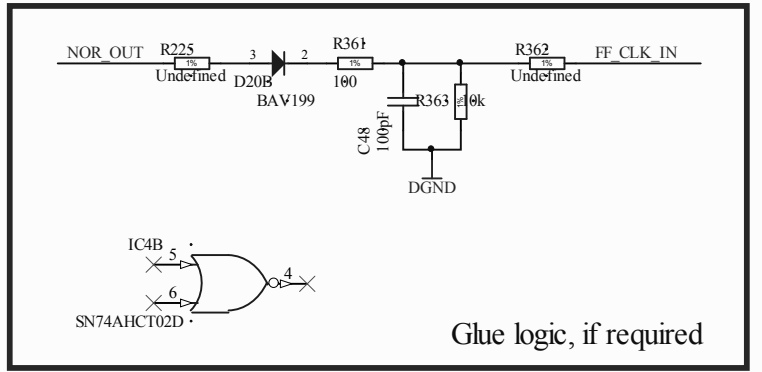
UP THR 2.437V - 1.741V  
 DOWN THR 2.35V - 1.63V  
 $f_{out}(150mA)=1.306MHz - 932kHz$



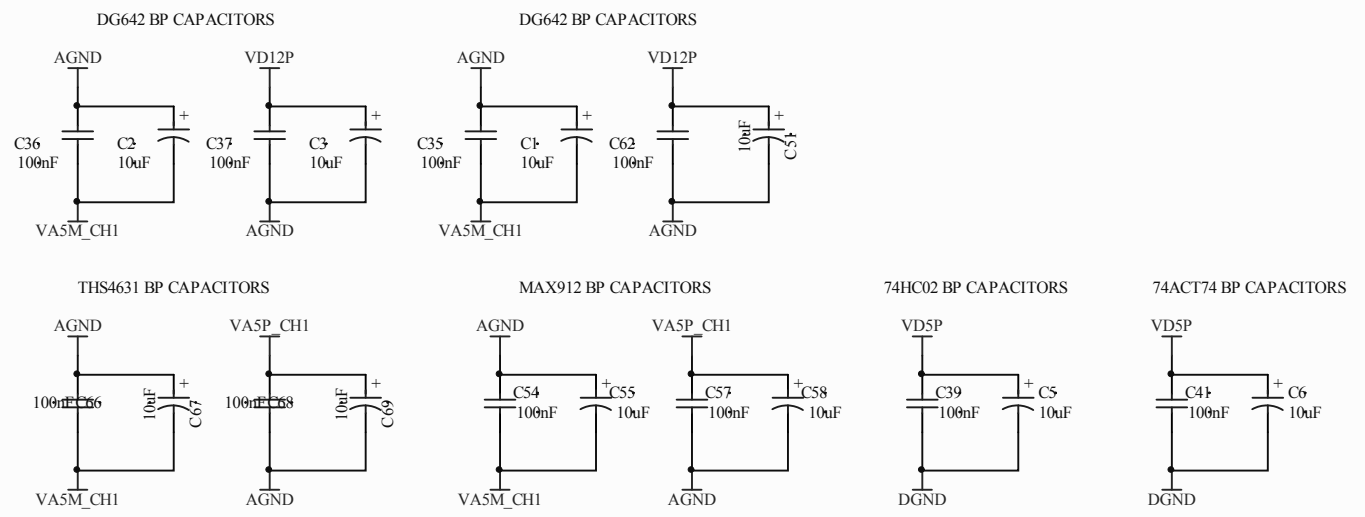
To be soldered to increase the maximum DC input current



To be soldered in alternative to DG642



Glue logic, if required



With ADG1436 the current limit is set by the OA (THS4631) and is equal to 150mA continuous

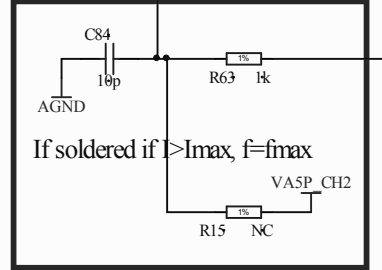
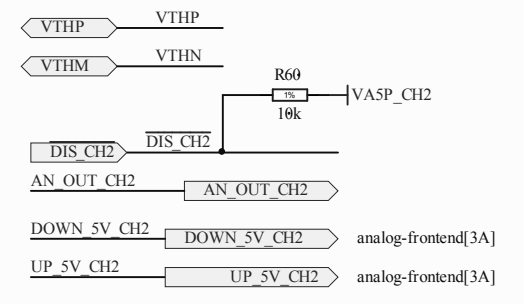
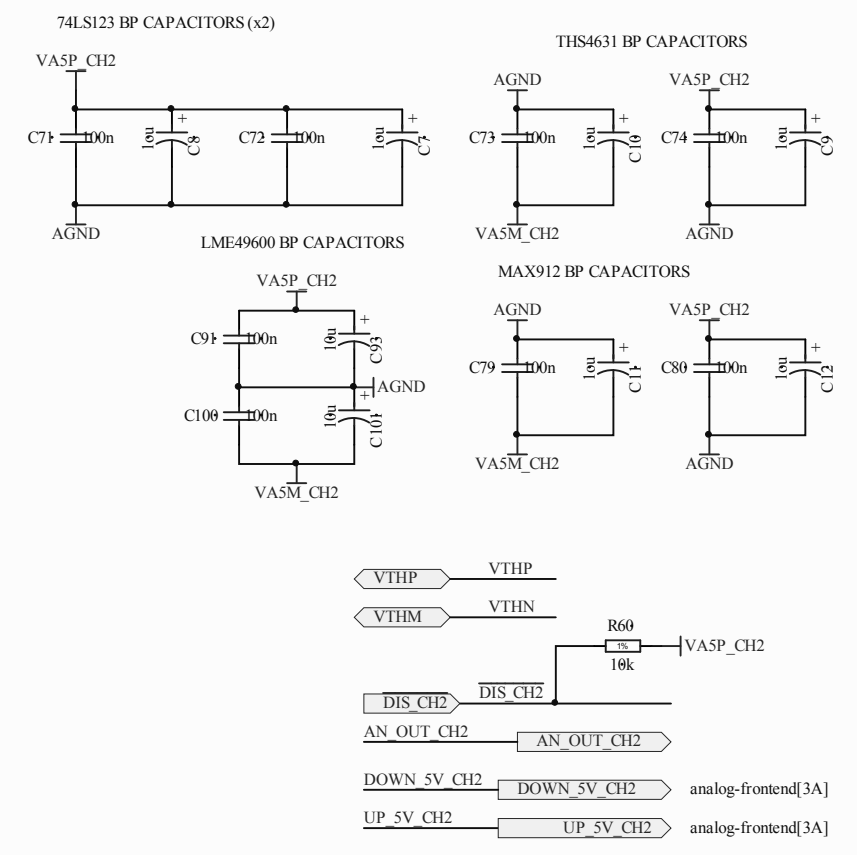
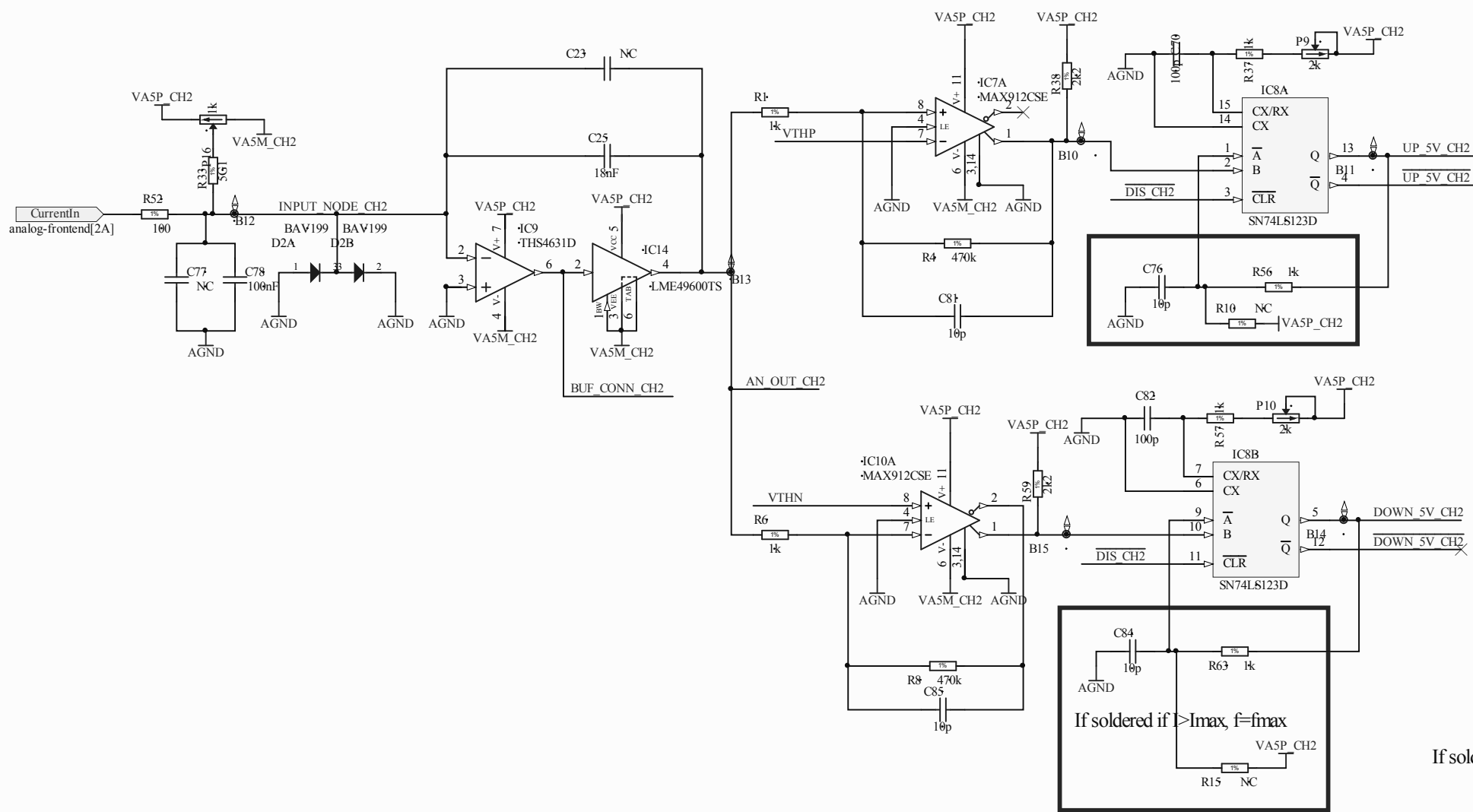
A precision adjustable voltage reference (LM385, 2%) is used to set the thresholds.

The input protection diodes can be changed or completely removed if the design targets at lower currents.

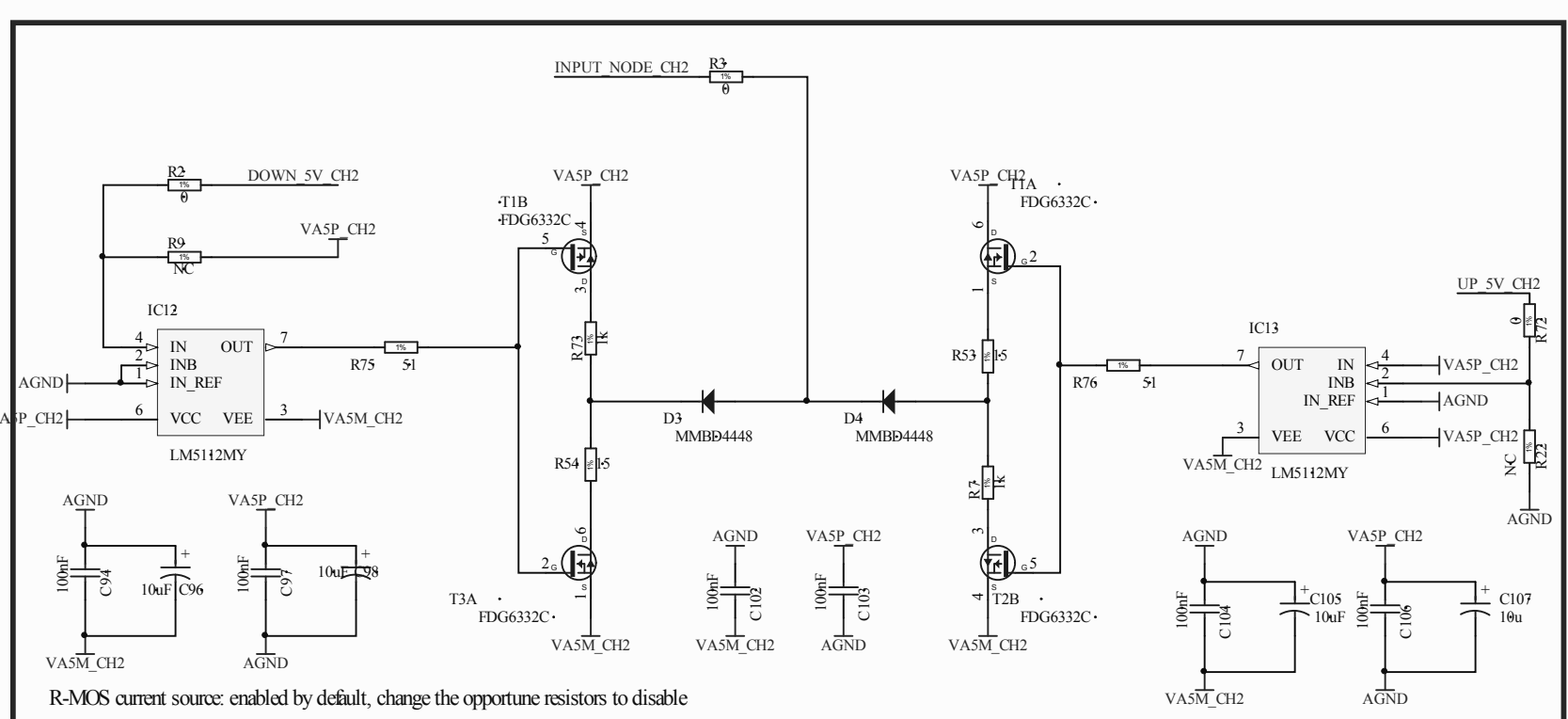
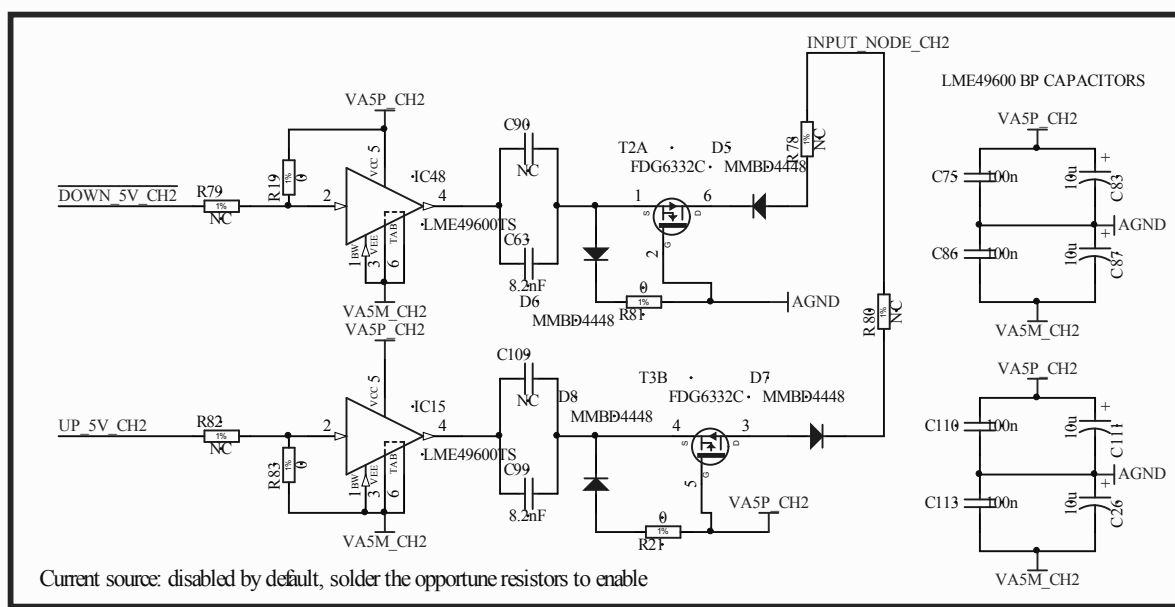
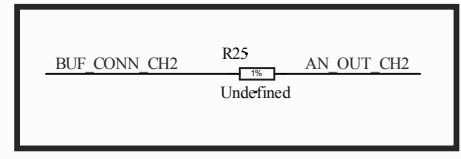
Each time one of the comparators trips, one of the capacitors is connected in the opposite direction and a charge equal to  $C \cdot V_{th}$  is removed.

The output frequency is given by:  $f_{out} = I / (2 \cdot C \cdot V_{th})$

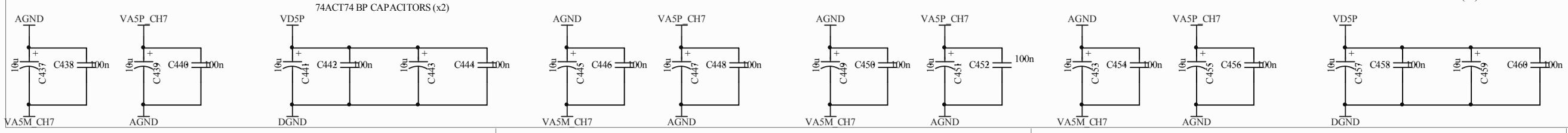
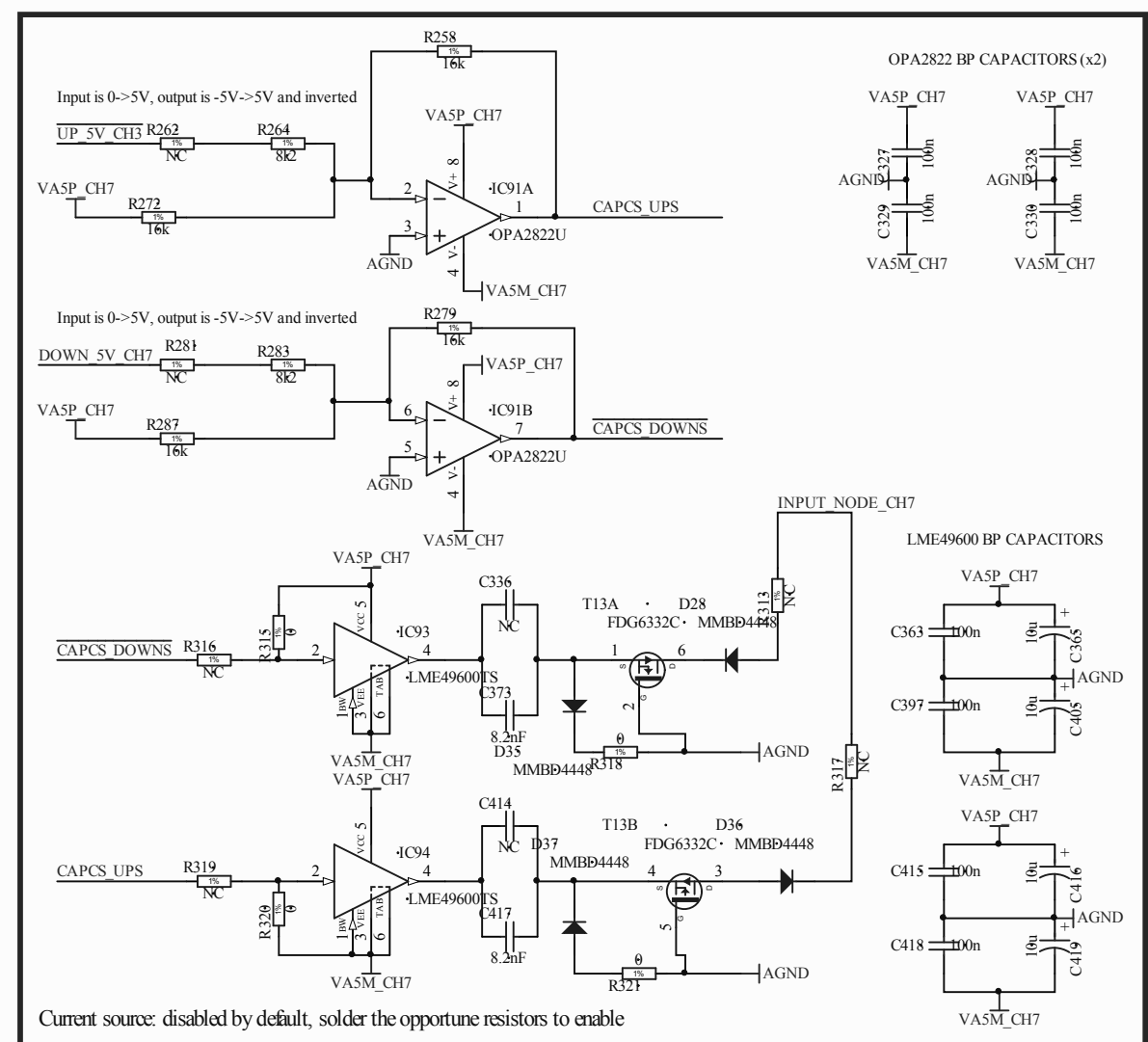
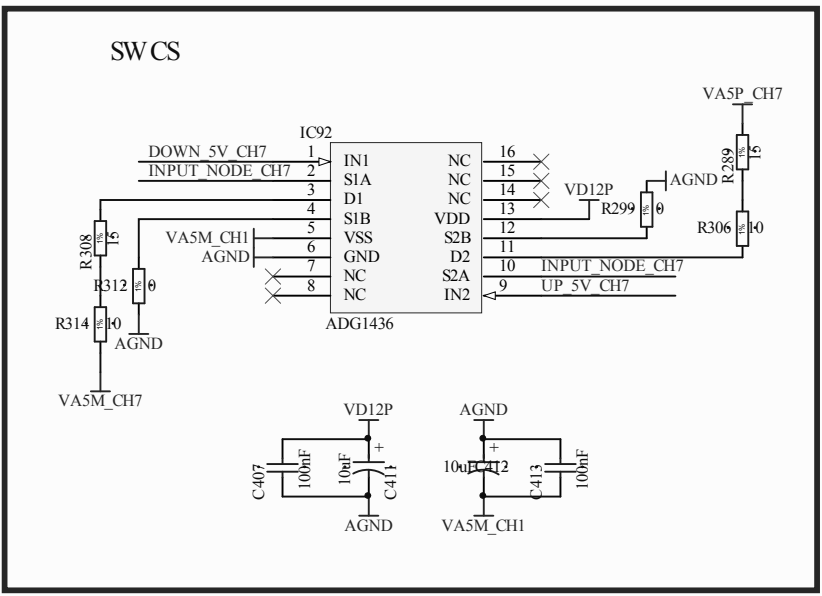
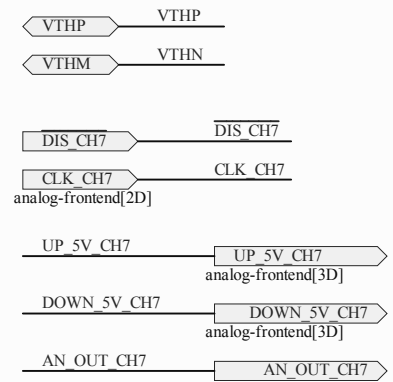
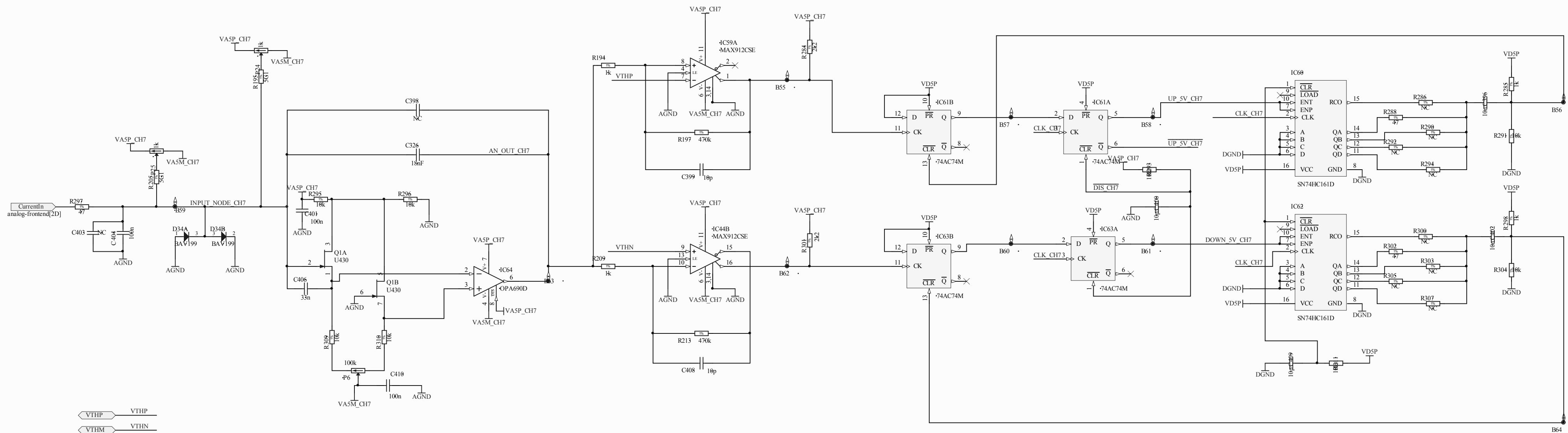
Projet/Equipement		-	
Document		-	
		<b>CFC - Test board</b> <b>CH1: SWCAP</b>	
Designer	Designer	XX/XX/XXXX	XX/XX/XXXX
Drawn by	Giuseppe G. Venturini	-	-
Check by	-	-	-
Last Mod.	-	-	11/30/2008
File	input-ch1.SchDoc	-	-
Print Date	12/1/2008 10:47:26 AM	Sheet	- of -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	Sub Rev A3 1



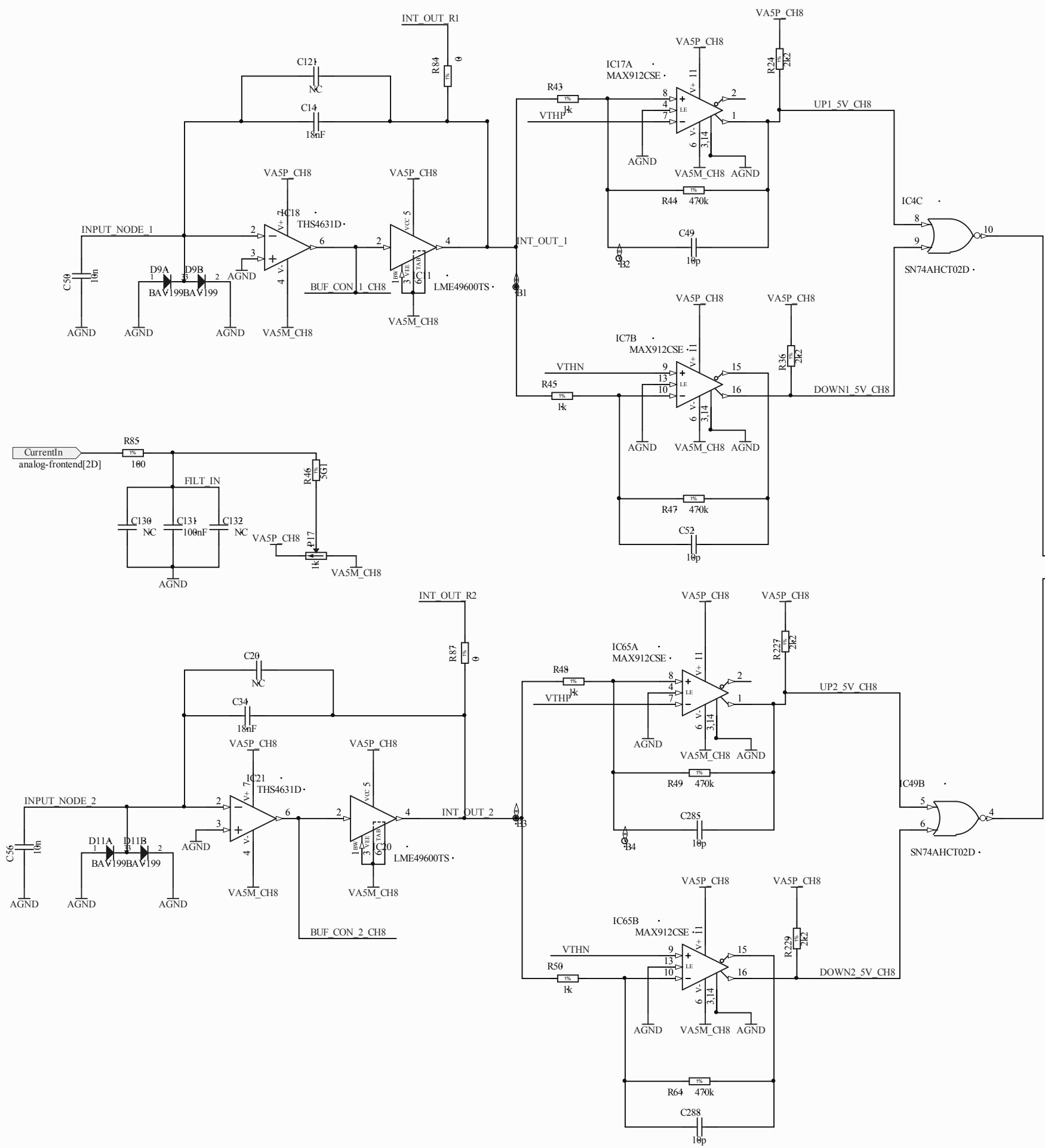
If soldered if  $I > I_{max}$ ,  $f = f_{max}$



Projet/Equipement		-	
Document		CFC - Test board CH2: ACB MOS/CAP	
Designer	Designer	XX/XX/XXXX	
Drawn by	Giuseppe G. Venturini	-	
Checkby	-	11/30/2008	
Last Mod.	-		
File	input-ch2.SchDoc		
Print Date	12/1/2008 10:47:40 AM	Sheet	- of -
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		Sub	Rev
		A3	1



Project/Equipment			
Document	CFC - Test board CH7: SCB IN-BUF MOS/CAP		
Designer	Designer	Checked by	XXXX/XXXX
File	input-ch7_SchDoc	Last Mod.	11/30/2008
Print Date	12/1/2008 10:47:54 AM	Sheet	of
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$$F_{out} = 1 / (C_{int} * V_{th})$$

