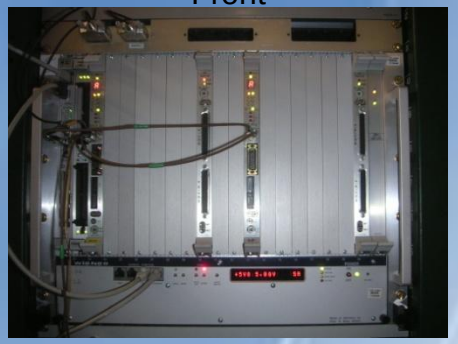
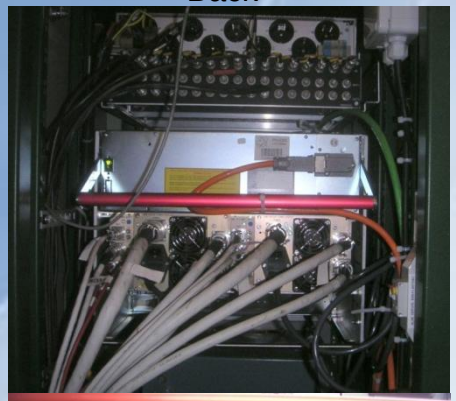
BLM and BWS installation examples

Front

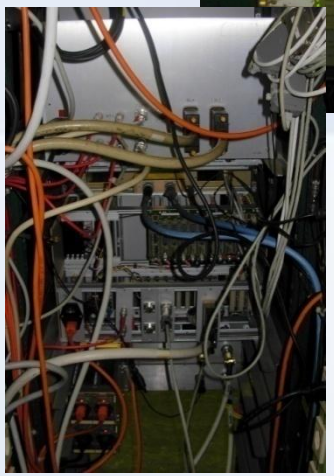


Back



BWS layout (pictures from the CPS)
Mix of analog, digital and supplies going through P2.
Installed in 2009. (**56 I/O through P2**)

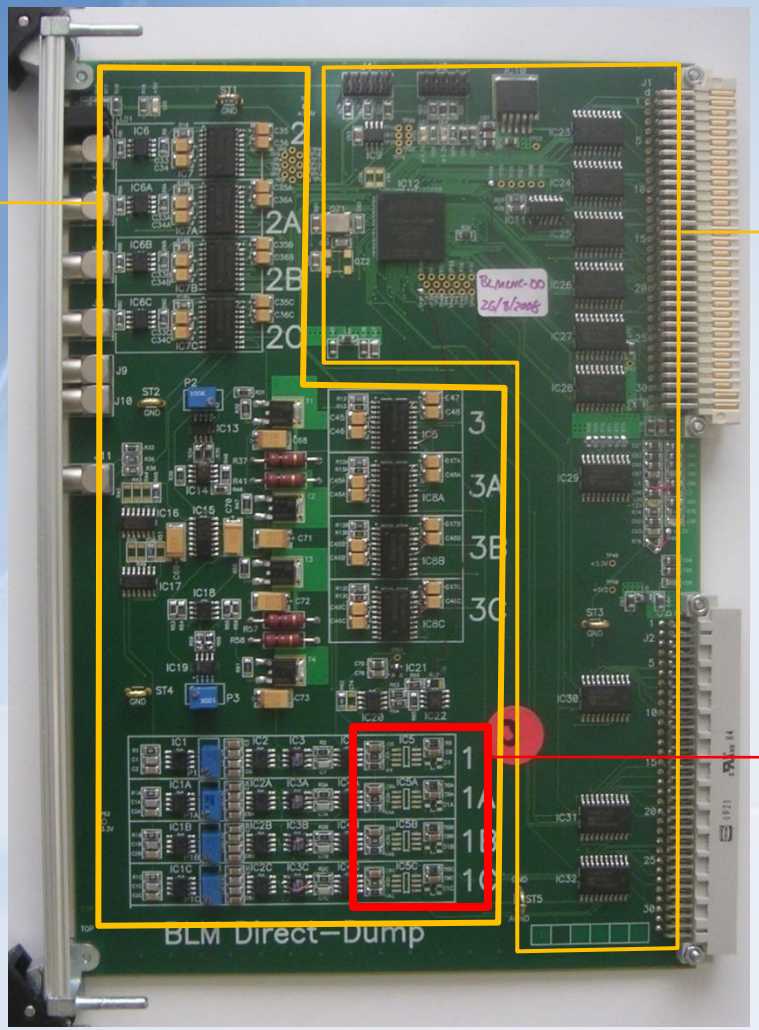
LHC BLM system: 4 crates connected through P2 connector (with the combiner card) for HV control, crate interconnections, beam permit and beam energy distribution. (**41 I/O through P2**)



SPS BLM system
(BA4 pictures)
(**> 40 I/O through P2**)

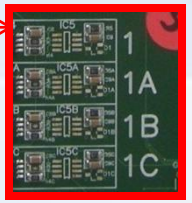
BLM LHC Direct - Dump

Analog Part



Digital Part

Signal conditioning was moved to the back of the VME and passing through P2, to improve signal/noise ratio and for safety reasons (avoiding risk of high voltage on the connector in case of malfunction of the IC)

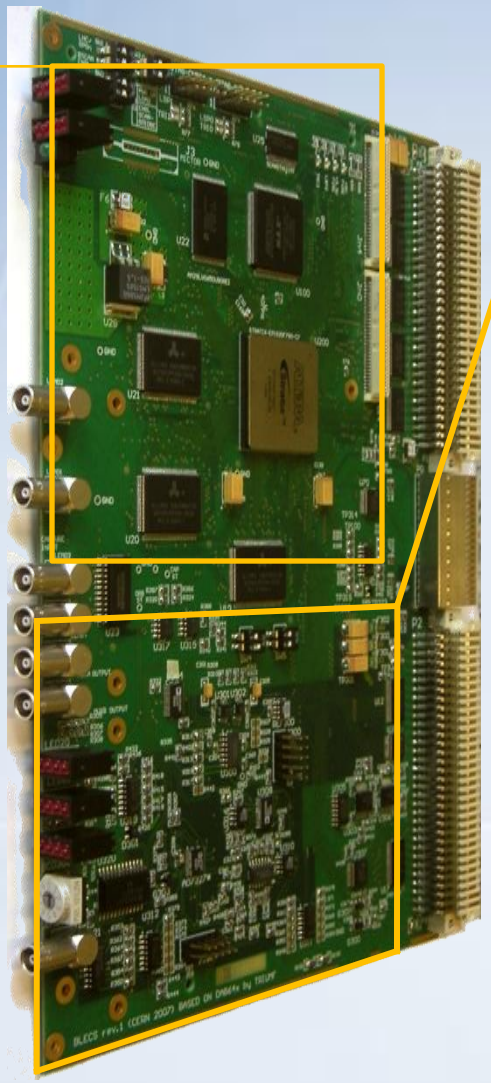


I/O through the P2 connector
4 analog signal inputs, 4 analog monitoring inputs

BLM LHC Combiner card

- Based on the DAB card
  => VME 64x
  => Stratix 40k
  => SRAM memory
  => One site code update
  => Specific BI signals on P0

- Reuse of existing material
  => FPGA code for
  VME
  Serial number chip
  Flash memory
  => Flash programming



Combiner features added.
Analog and digital control.
all going through P2 connector

- Beam permit
  => Daisy chain between crates
  => Beam Interlock
  CIBUS interface

- Interface to high voltage PS
  DAC for control
  ADC for monitoring

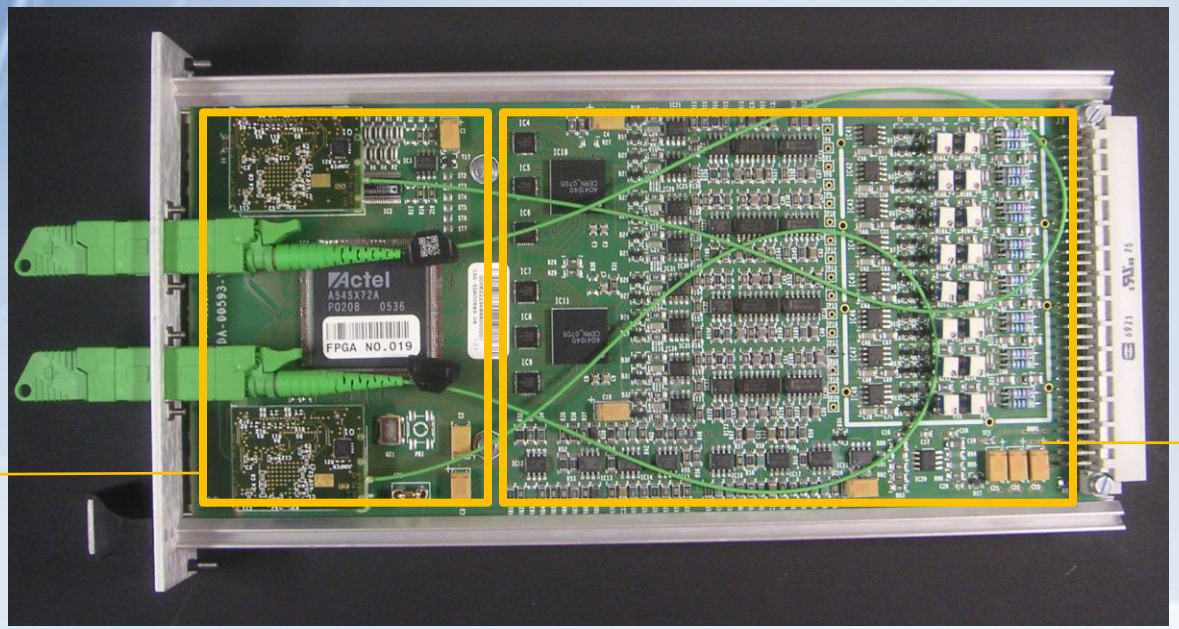
- Monitoring VME PS
  for specific behavior (ripples)

- Crate interconnections for
  test of the BLM system

41 I/O through the P2 connector

BLM LHC tunnel card (example of analog & digitalisation circuit)

Digital Part:
Processing
& Optical
Transmission

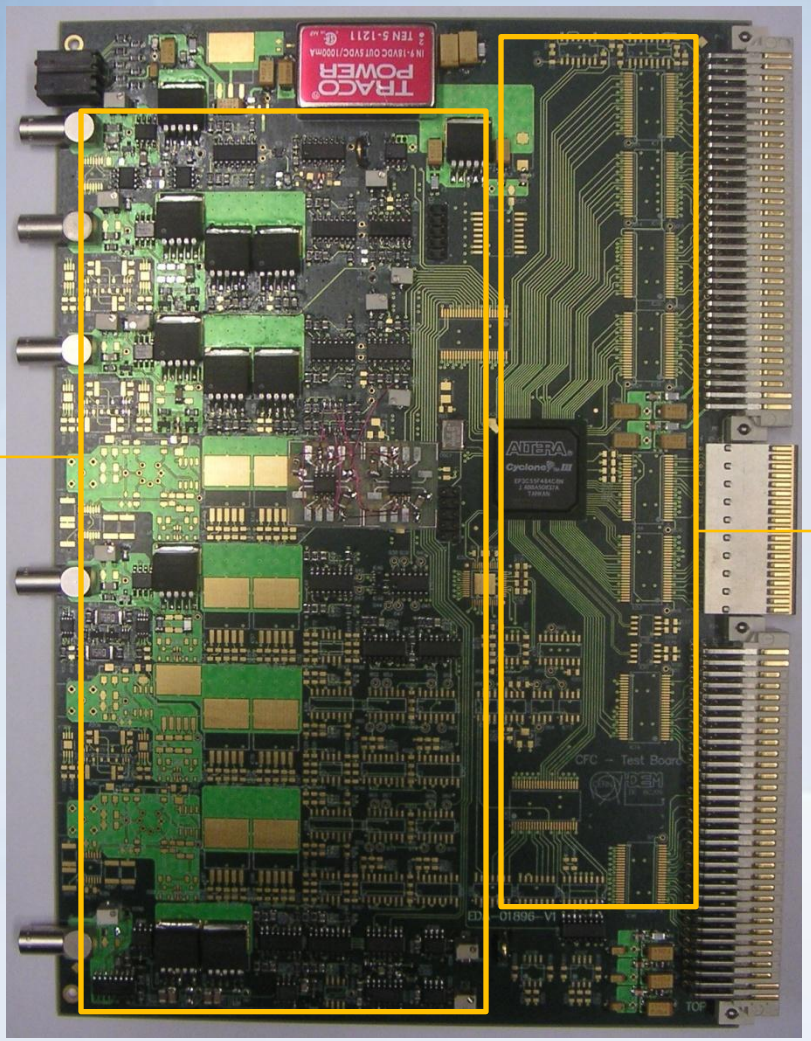


Analog Part:
Current measurements
with CFC circuit +
digitalisation
8 inputs
Dynamic : 10^8

For the LHC, one surface electronic board BLETC (DAB+Mezzanine) handles 2 of this cards (16 BLM channels in total)

BLM CPS prototype

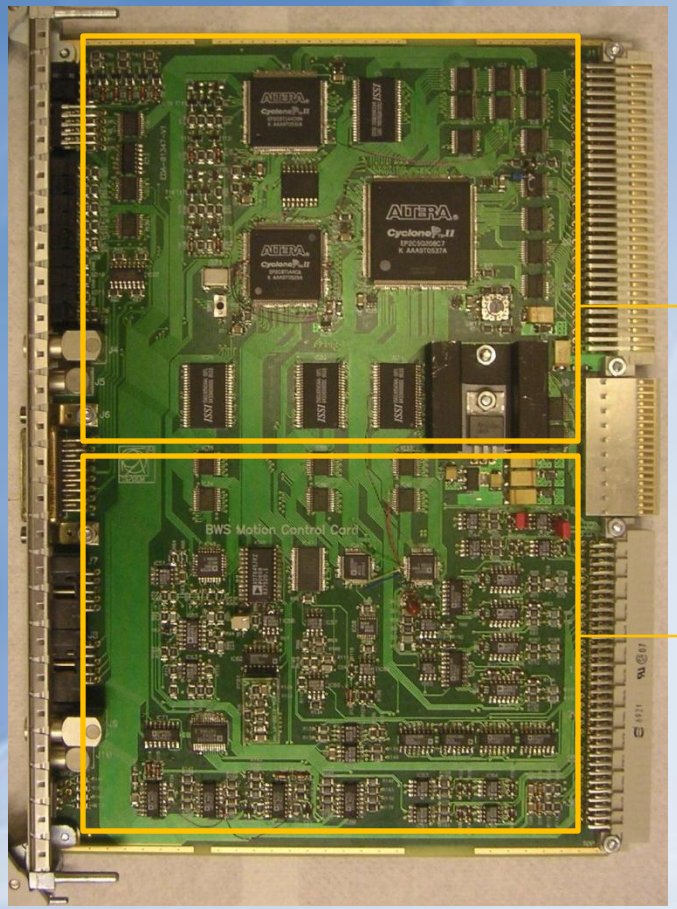
Analog Part.
Different circuit architectures are being tested for measuring 1nA-100mA (8 orders) on 8 channels



Digital Part

I/O through the P2 connector not defined yet

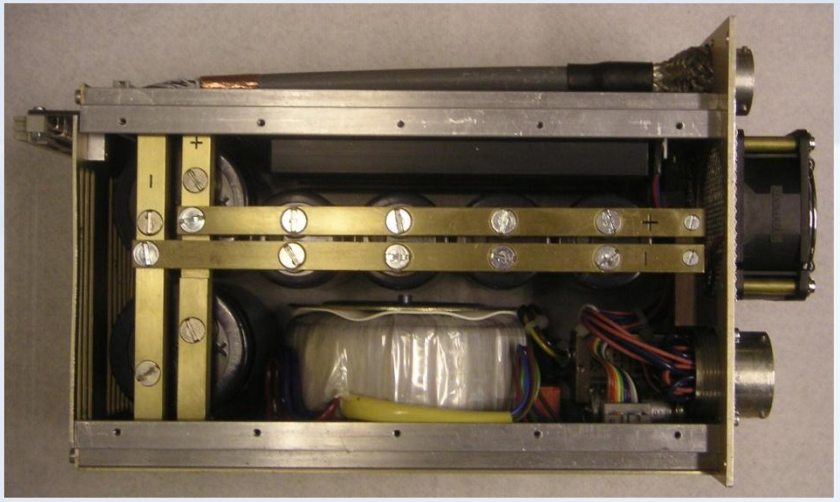
BWS motion control (All machines)



Digital part:
3 Altera FPGA
SRAM memory
Specific BI signals on P0
Direct access to DAC and ADC
with the CPU

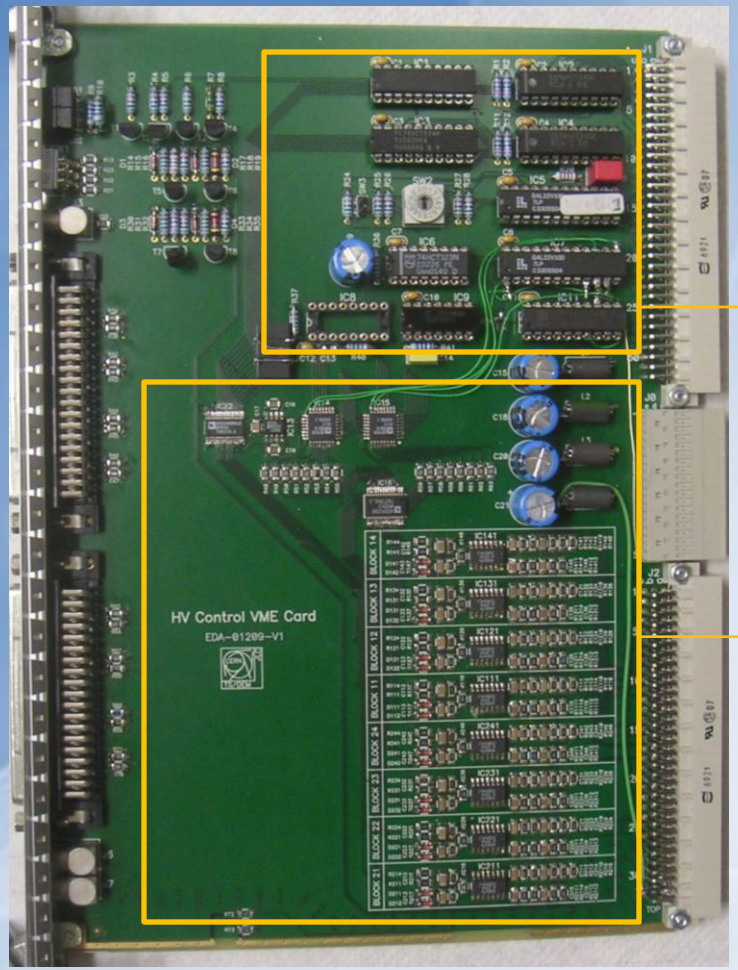
Analog from/to digital conversions
Signal conditioning
Analog powering
Threshold comparison for status
Analog feedback loop
All through P2 connector to power amplifier

56 I/O through P2



BWS power amplifier is plugged directly on the back of the crate

BWS HV control card (All machines)

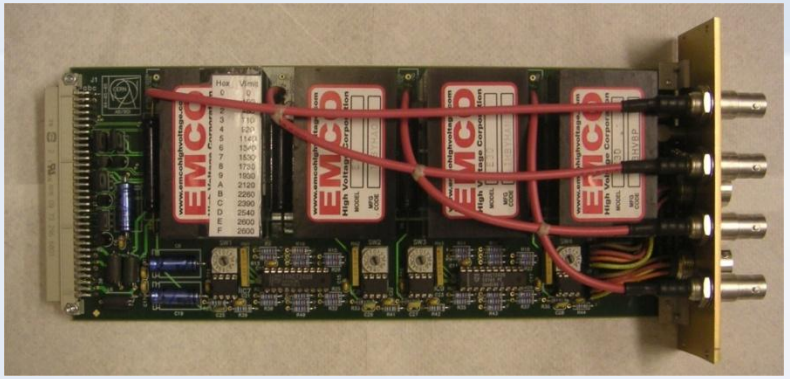


Digital part

Analog part:
ADC and DAC
Signal conditioning
Option to extend through the FP

Control of 4 HV modules with
Monitoring of I and V
28 I/O through the P2 connector

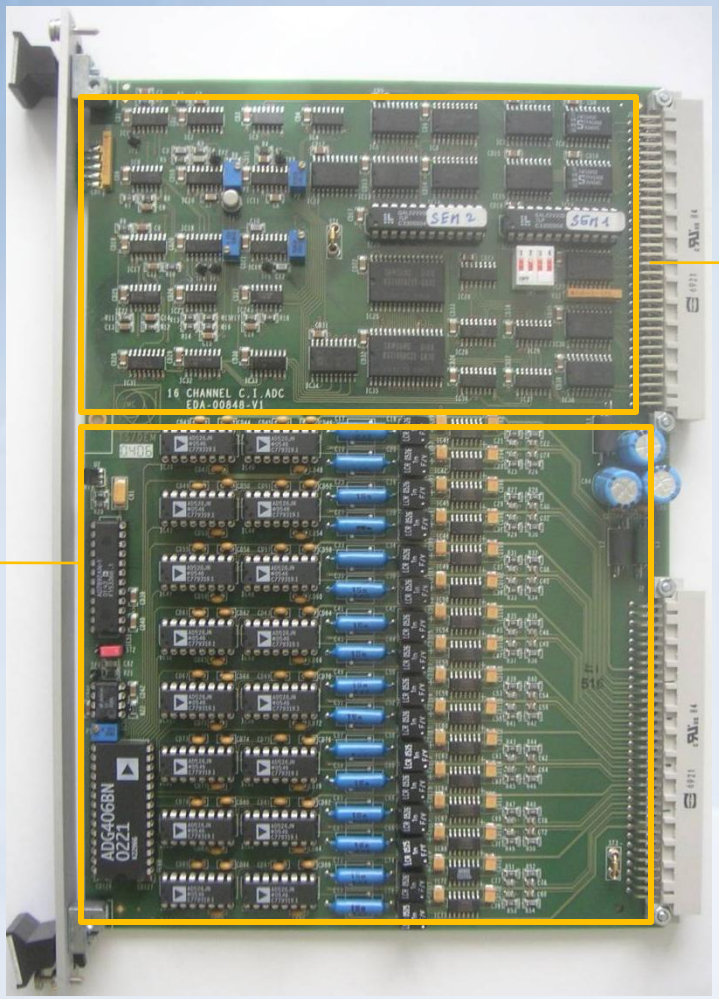
BWS HV module is plugged
directly on the back of the crate



SEM 16 channels C.I. ADC (SPS)

Digital Part

Analog Part:
16 channels
Dynamic > 10^6



16 analog signals through the P2 connector

KEY POINTS

- In all designs the analog part is occupying 40%-70% of the boards area.
  - Size doesn’t fit in the small FMC mezzanines.
  - Some circuits needs to dissipate some power.

- Almost each design uses the P2 connector.
  - For signal and control connections to the outside.
  - To avoid cabling in the front of the crates or patch panels.
  - Easy exchange of the cards, no cable mix up.

- Noise and EMC issues.
  - Low noise analog voltages usually needed: ±15V, +5V
  - Proximity of high speed digital circuits to the high sensitivity inputs of the amplifiers to be avoided.

Proposal for P2 pinout to use the back of the VME

VME64 P2 Connector:
Raw A, C, D, Z: **110 lines** of UsrDef

VME64x P2 Connector					
Pin	Signal Name Row z	Signal Name Row A	Signal Name Row B	Signal Name Row C	Signal Name Row d
1	UsrDef	UsrDef	+5V	UsrDef	UsrDef
2	GND	UsrDef	GND	UsrDef	UsrDef
3	UsrDef	UsrDef	RETRY	UsrDef	UsrDef
4	GND	UsrDef	A24	UsrDef	UsrDef
5	UsrDef	UsrDef	A25	UsrDef	UsrDef
6	GND	UsrDef	A26	UsrDef	UsrDef
7	UsrDef	UsrDef	A27	UsrDef	UsrDef
8	GND	UsrDef	A28	UsrDef	UsrDef
9	UsrDef	UsrDef	A29	UsrDef	UsrDef
10	GND	UsrDef	A30	UsrDef	UsrDef
11	UsrDef	UsrDef	A31	UsrDef	UsrDef
12	GND	UsrDef	GND	UsrDef	UsrDef
13	UsrDef	UsrDef	+5V	UsrDef	UsrDef
14	GND	UsrDef	D16	UsrDef	UsrDef
15	UsrDef	UsrDef	D17	UsrDef	UsrDef
16	GND	UsrDef	D18	UsrDef	UsrDef
17	UsrDef	UsrDef	D19	UsrDef	UsrDef
18	GND	UsrDef	D20	UsrDef	UsrDef
19	UsrDef	UsrDef	D21	UsrDef	UsrDef
20	GND	UsrDef	D22	UsrDef	UsrDef
21	UsrDef	UsrDef	D23	UsrDef	UsrDef
22	GND	UsrDef	GND	UsrDef	UsrDef
23	UsrDef	UsrDef	D24	UsrDef	UsrDef
24	GND	UsrDef	D25	UsrDef	UsrDef
25	UsrDef	UsrDef	D26	UsrDef	UsrDef
26	GND	UsrDef	D27	UsrDef	UsrDef
27	UsrDef	UsrDef	D28	UsrDef	UsrDef
28	GND	UsrDef	D29	UsrDef	UsrDef
29	UsrDef	UsrDef	D30	UsrDef	UsrDef
30	GND	UsrDef	D31	UsrDef	UsrDef
31	UsrDef	UsrDef	GND	UsrDef	GND
32	GND	UsrDef	+5v	UsrDef	VPC

L. Davis

- Analog power supplies:

1) (BI type A) 5V, -5.2V, -2V or (BI type B) ±15V, 5V from P0.
See EDMS No: 365170 LHC instrumentation VME crates.
2) ±12V from P1 connector could be considered as analog, but with common ground with the other voltages?
3x (3 PS + 3 return) + 3x(2 PS) = **24 lines**

- Digital supplies from the VME 3.3V (5V already there). **3 lines**

- Timing signals from PLL and/or P0? 4 LVDS, **8 lines**

- Standard clock lines from/to the FPGA. **3 lines**

- I/O to the FPGA for digital control and data transmissions
(Fast ADC/DAC, serial link, digital control)
Max signal speed achievable ? Some high speed ?
17 LVDS, **34 lines**

- I/O to FMC mezzanine(s)
(in case of no signal conditioning before P2 connector)
16 lines (8 LVDS?) + 8 analog lines = **24 lines**

TOTAL : 96 lines + 14 GND / AGND = 110 lines