Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	Bus line-0	-5V2RET	-5V2RET	HW Low Byte 1 bit 0	HW High Byte 1 bit 0	GND
2	GND	Bus line-1	-5V2RET	-5V2RET	HW Low Byte 1 bit 1	HW High Byte 1 bit 1	GND
3	GND	Bus line-2	-5V2RET	-5V2RET	HW Low Byte 1 bit 2	HW High Byte 1 bit 2	GND
4	GND	Bus line-3	-5V2	-5V2	HW Low Byte 1 bit 3	HW High Byte 1 bit 3	GND
5	GND	Bus line-4	-5V2	-5V2	HW Low Byte 1 bit 4	HW High Byte 1 bit 4	GND
6	GND	Bus line-5	-5V2	-5V2	HW Low Byte 1 bit 5	HW High Byte 1 bit 5	GND
7	GND	Bus line-6	-2VRET	-2VRET	HW Low Byte 1 bit 6	HW High Byte 1 bit 6	GND
8	GND	Bus line-7	-2VRET	-2VRET	HW Low Byte 1 bit 7	HW High Byte 1 bit 7	GND
9	GND	GPPL-0	-2V	-2V	Daisy chain1 - 1-in	Daisy chain1 -1-out	GND
10	GND	GPPL-1	-2V	-2V	Daisy chain 1-2-in	Daisy chain 1-2-out	GND
11	GND	GPPL-2	GPPL-3	GPPL-4	GPPL-5	GPPL-6	GND
12	GND	Bus line1-0	+5V	+5V	Bunch Select 1 Bit 0	LVDS Turn clock Delay 1 +	GND
13	GND	Bus line1-1	+5V	+5V	Bunch Select 1 Bit 1	LVDS Turn clock Delay 1 -	GND
14	GND	Bus line1-2	+5VRET	+5VRET	Bunch Select 1 Bit 2	TTL Turn clock Delay 1 +	GND
15	GND	Bus line1-3	+5VRET	+5VRET	Bunch Select 1 Bit 3	TTL Turn clock Delay 1 -	GND
16	GND	Bus line1-4	+15V	+15V	Bunch Select 1 Bit 4	LVDS 40 MHz Clock 1 +	GND
17	GND	Bus line1-5	+15VRET	+15VRET	Bunch Select 1 Bit 5	LVDS 40 MHz Clock 1 -	GND
18	GND	Bus line1-6	-15VRET	-15VRET	Bunch Select 1 Bit 6	TTL 40 MHz Clock 1 +	GND
19	GND	Bus line1-7	-15V	-15V	Bunch Select 1 Bit 7	TTL 40 MHz Clock 1 -	GND

Table 6a: Pin allocations on J0 for slots 3 to 11 (Front view)

Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	Bus line-0	-5V2RET	-5V2RET	HW Low Byte 2 bit 0	HW High Byte 2 bit 0	GND
2	GND	Bus line-1	-5V2RET	-5V2RET	HW Low Byte 2 bit 1	HW High Byte 2 bit 1	GND
3	GND	Bus line-2	-5V2RET	-5V2RET	HW Low Byte 2 bit 2	HW High Byte 2 bit 2	GND
4	GND	Bus line-3	-5V2	-5V2	HW Low Byte 2 bit 3	HW High Byte 2 bit 3	GND
5	GND	Bus line-4	-5V2	-5V2	HW Low Byte 2 bit 4	HW High Byte 2 bit 4	GND
6	GND	Bus line-5	-5V2	-5V2	HW Low Byte 2 bit 5	HW High Byte 2 bit 5	GND
7	GND	Bus line-6	-2VRET	-2VRET	HW Low Byte 2 bit 6	HW High Byte 2 bit 6	GND
8	GND	Bus line-7	-2VRET	-2VRET	HW Low Byte 2 bit 7	HW High Byte 2 bit 7	GND
9	GND	GPPL-0	-2V	-2V	Daisy chain 2- 1-in	Daisy chain 2-1-out	GND
10	GND	GPPL-1	-2V	-2V	Daisy chain 2- 2-in	Daisy chain 2- 2-out	GND
11	GND	GPPL-2	GPPL-3	GPPL-4	GPPL-5	GPP-6	GND
12	GND	Bus line2-0	+5V	+5V	Bunch Select 2 Bit 0	LVDS Turn clock Delay 2 +	GND
13	GND	Bus line2-1	+5V	+5V	Bunch Select 2 Bit 1	LVDS Turn clock Delay 2 -	GND
14	GND	Bus line2-2	+5VRET	+5VRET	Bunch Select 2 Bit 2	TTL Turn clock Delay 2 +	GND
15	GND	Bus line2-3	+5VRET	+5VRET	Bunch Select 2 Bit 3	TTL Turn clock Delay 2 -	GND
16	GND	Bus line2-4	+15V	+15V	Bunch Select 2 Bit 4	LVDS 40 MHz Clock 2 +	GND
17	GND	Bus line2-5	+15VRET	+15VRET	Bunch Select 2 Bit 5	LVDS 40 MHz Clock 2 -	GND
18	GND	Bus line2-6	-15VRET	-15VRET	Bunch Select 2 Bit 6	TTL 40 MHz Clock 2 +	GND
19	GND	Bus line2-7	-15V	-15V	Bunch Select 2 Bit 7	TTL 40 MHz Clock 2 -	GND

Table 6b: Pin allocations on J0 for slots 13 to 21 (Front view)