Results of a radiation damage test for **PAMELA**

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The experiment **PAMELA**, devoted to study the energy spectra of cosmic rays (with emphasis on positrons, antiprotons and eventually antinuclei), is scheduled to be launched at the end of 2002 from the Cosmodrome of Baykonur (Kazakhstan). It will be carried on the satellite Resurs-DK1, manufactured by TsSKB-Progress in Samara (Russia), and devoted to Earth observation. The satellite will fly on a quasi-polar orbit with a maximum height of 600 km, and its lifetime will be three years.

In a space mission as such, micro-electronic devices are subject to interaction with highly ionizing particles, like high-Z, low-energy nuclei. These interactions can result in the so-called ***SEE*** (Single Event Effects), like ***SEL*** (Single Event Latch-up) and ***SEU*** (Single Event Upset). A ***SEE*** is a change in a microelectronic device caused by being hit by a single energetic particle. A ***SEU*** occurs when an energetic particle passing through a digital electronic device causes an unplanned change in its logic state. Afterward, the device may be re-written into the intended state. In the case of a ***SEL*** the device is latched into one logic state and will not change states in response to a logic signal. This occurs when the ***SEU*** activates a parasitic circuit in the device which connects its power supply to ground. If the current is externally limited, no permanent damage occurs and the operability of the device can be recovered by cycling the power.

To ensure that a micro-electronic device is qualified for surviving in space, it must undergo a beam test that can simulate these interactions. The critical parameter for these tests is the ionization energy loss per depth, known as ***LET*** (Linear Energy Transfer), usually measured in MeV/(mg/cm^2). Purpose of the test is to determine the ***SEE*** cross-section of the ***DUT*** (Device Under Test) as a function of the ***LET***

$$\sigma_{\boldsymbol{SEE}} = f(\boldsymbol{LET})$$

If the irradiation occurs during a time ΔT, for a given $\boldsymbol{LET}$, the relationship between cross-section and number of occurred $\boldsymbol{SEE}$ is

$$\sigma_{\boldsymbol{SEE}} = \frac{N_{\boldsymbol{SEE}}}{\Phi_{\Delta T}(\boldsymbol{LET})}$$

where $\Phi_{\Delta T}(\boldsymbol{LET})$ is the integrated fluence of ions per cm^2. Assuming an uniform distribution of particles in the beam, then

$$\Phi_{\Delta T}(\boldsymbol{LET}) = \frac{N_{beam}}{S_{beam}} \Delta T$$

where S_{beam} is the beam section and N_{beam} is the total number of particles in the beam per second.

The test was performed at the accelerator facility of the High-Energy Laboratory at the Joint Institute for Nuclear Research in Dubna (Russia), in December 8th to 10th, 2001. For both tests, a 150 MeV/n beam of ^{24}Mg ions extracted from the NUCLOTRON accelerator was employed. The extracted beam, after passing through a thin (80 μm) Ti window, is collimated to a diameter of 12 mm, by a hole in a 5 cm thick Pb brick. The section of the extracted beam was photographed before and after collimation (see fig. 1). At the exit window of the collimator, a 5 mm thick plastic scintillator was placed to count the incoming flux of particles on our $\boldsymbol{DUT}$, which was placed approx. 20 cm downstream. The $\boldsymbol{LET}$ has been evaluated with the SRIM simulation package. For all tests we obtained

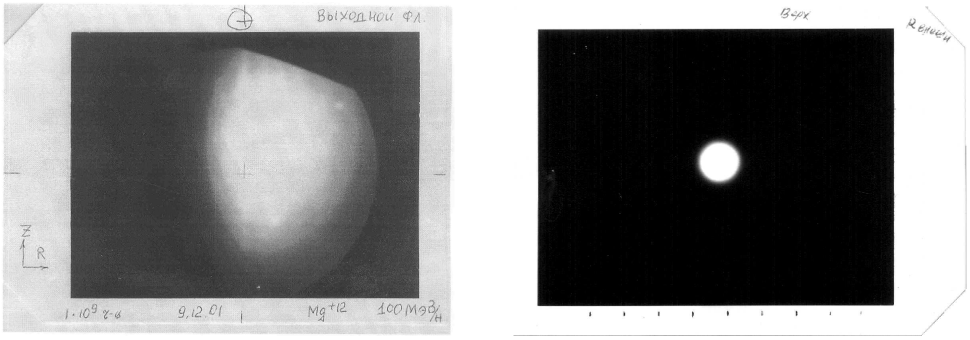

Figure 1: The beam before (left) and after (right) collimation.

$$\begin{aligned}
N_{beam} \cdot \Delta T &= 3 \cdot 10^7 \text{particles} \\
S_{beam} &= 1.13 \text{ cm}^2 \\
\Phi_{\Delta T}(\boldsymbol{LET}) &= 2.7 \cdot 10^7 \text{particles/cm}^2 \\
\boldsymbol{LET} &= 0.74 \text{ MeV/(mg/cm}^2)
\end{aligned}$$

For all successfully tested devices (no ***SEE*** detected), we can thus establish only an upper limit for the ***SEE*** cross-section, that is

$$\sigma_{\boldsymbol{SEE}} < 1 \cdot 10^{-7}\ \mathrm{cm}^2/\mathrm{device}$$

The first ***DUT*** was a 1 Mbit Flash Memory, manufactured by ST, mod. M25P10. For test purpose only, the ***DUT*** was mounted as a "piggy-back" on a custom made DAQ board manufactured by CAEN (Italy). The DAQ board is equipped with a DSP from Analog Devices, mod. ADSP2187. Communication to and from our PC and the DAQ board was ensured by a serial cable. The board was supplied at +5 V. To test for ***SEU*** the whole memory was filled with a known pattern of '0' and '1', and then continuously read during irradiation. In case of change of a memory cell content,this was re-written, and a ***SEU*** counter updated. For ***SEL*** test, the DSP monitors the current of the chip: if it exceeds a given threshold (50 mA), the power is cut out from the chip, a ***SEL*** counter is updated and the chip restarted. Two identical chips were tested, and no ***SEU*** or ***SEL*** occurred in both of them.

The second part of the test was performed on two DC/DC converters, manufactured by CAEN. Both were supplied at +20 V. The two devices were tested only for ***SEL***, continuously monitoring their output voltage during the irradiation. The first DC/DC converter, mod. S9006, has an output voltage of +3.4 V, and it was irradiated on 7 spots, corresponding to 8 chips. The second DC/DC converter, mod. S9004, has an output voltage of +5.6 V, and it was irradiated on 6 spots, corresponding to 7 chips. The last tested chip (a power MOSFET) on the first DC/DC converter had a failure (probably a gate rupture) and functionality of the DC/DC converter could not be restored even after power cycling. The other chips survived the test.