The LHC Beam Loss Monitoring System's Real-Time Data Analysis Card

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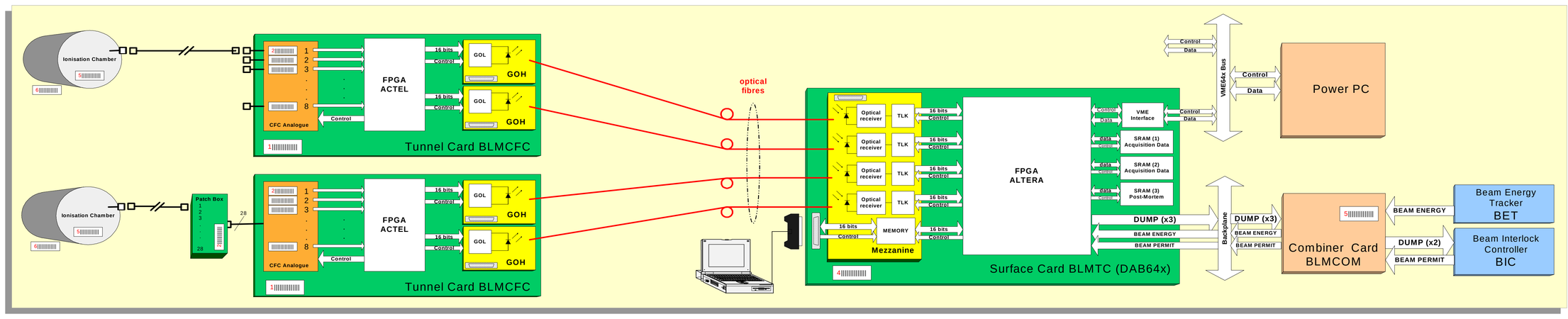
Abstract: The *BLM* (Beam Loss Monitoring) system has to prevent the superconducting magnets from being quenched and protect the machine components against damages making it one of the most critical elements for the protection of the LHC. The complete system consists of 3600 detectors, placed at various locations around the ring, tunnel electronics, which are responsible for acquiring, digitising, and transmitting the data, and surface electronics, which receive the data via 2km optical data links, process, analyze, store, and issue warning and abort triggers. At those surface units, named *BLMTCs*, the backbone on each of them is an *FPGA* (field programmable gate array) which treats the loss signals collected from 16 detectors. It takes into account the beam energy and keeps 192 running sums giving loss durations of up to the last 100 seconds before it compares them with thresholds uniquely programmable for each detector. In this paper, the *BLMTC's* design is explored giving emphasis to the strategies followed in combining the data from the integrator and the *ADC*, and in keeping the running sums updated in a way that gives the best compromise between memory needs, computation, and approximation error.

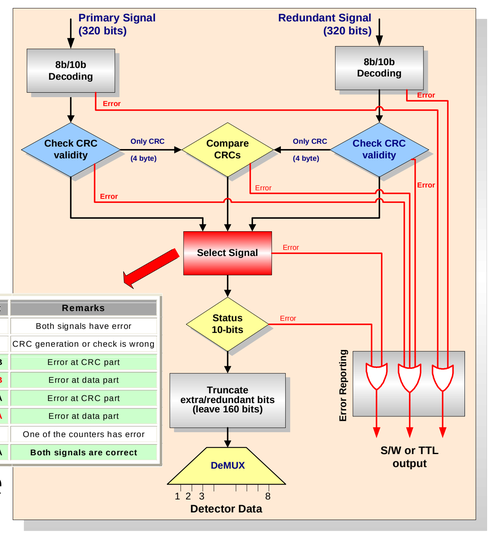
BLM System Overview



Around 3600 *Ionization Chambers* are the detectors of the system. A bunch of up to 8 of them can be connected to each of the tunnel cards. In those tunnel cards, called *BLMCFCs*, an *Actel FPGA* acquires and digitises the data from the detectors using *CFCs* and *ADCs* and transmits those at the surface using *Gigabit Optical Links*. There, the data analysis cards, named *BLMTCs*, receive those data and an *Altera Stratix FPGA* decides whether or not a dump request should be initiated. Each surface card receives data from 2 tunnel cards, which means that it can treat up to 16 channels simultaneously.

Transmission Check

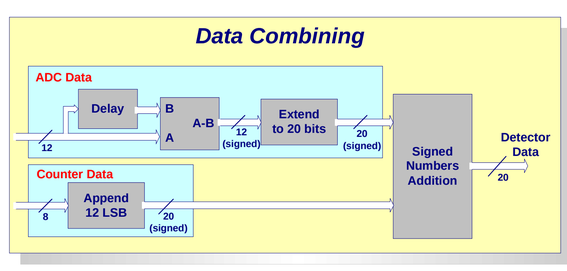
In the *BLMTC* design in order to increase the reliability of the communication link it was decided to double it. A comparison of the two can be made and in the case of a difference to trigger a dump of the beam. The *CRC* (Cyclic Redundancy Check), a polynomial arithmetic based algorithm, is widely used as error detection scheme. Here, the redundant bits it introduces are not only used to detect transmission but also the difference between the two signals.



CRC A	CRC B	Compare	Output	Remarks
Error	Error	Error	Dump	Both signals have error
Error	Error	OK	Dump	CRC generation or check is wrong
Error	OK	Error	Signal B	Error at CRC part
Error	OK	OK	Signal B	Error at data part
OK	Error	Error	Signal A	Error at CRC part
OK	Error	OK	Signal A	Error at data part
OK	OK	Error	Dump	One of the counters has error
OK	OK	OK	Signal A	Both signals are correct

The "*Signal Select*" Block has the responsibility of selecting the error free signal to convey on the stages below and in addition increases the availability of the system using efficiently all information. Finally, in some cases it can also indicate problematic areas in the tunnel installation.

CFC & ADC Data Combining



Based on the fact that the two types of data acquired for each detector are different, a pre-processing is needed in order those to be combined seamlessly.

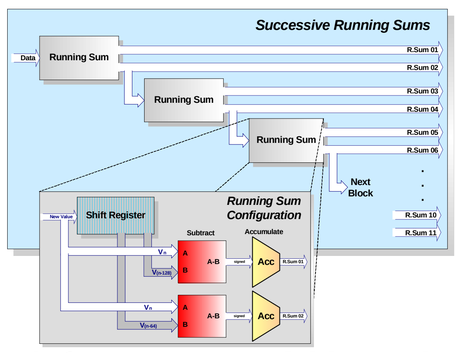
The measurement of the frequency produced by the *Current-to-Frequency Converter* with a counter relates to the current accumulated between the last acquisitions. On the other hand, the voltage measured by the *ADC* is the fraction remained between two counts.

In order to combine those data the difference of the last two *ADC* measurements, which then corresponds to the counter fraction of the last 40 us, should be added to the counter value. Of course, since the difference could be a negative number signed number arithmetic is used for the addition.

Using this scheme, the usage of resources and computation effort is minimised and all later stages are exploiting those combined values.

Successive Running Sums

The *Running Sums* can be produced simply by adding the newly acquired value to a register and subsequently subtracting from it a value coming delayed by a number of cycles in a shift register.



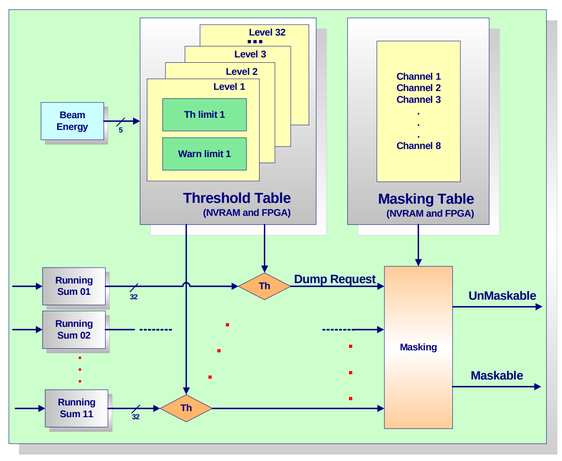
A similar configuration is used in the *BLMTC* where, in order to increase the efficiency in resources, it is making use of the multipoint shift registers available on the *Stratix* devices and it is adding the difference of those two values to an *Accumulator*.

	Time windows		Refreshing		Shift Register Name	Signal Name	bits used for each detector
	40 µs steps	ms	40 µs steps	ms			
System A	1	0.04	1	0.04		RS0	18
	2	0.08	1	0.04		RS1	22
	8	0.32	1	0.04	SR1	RS2	22
	16	0.64	1	0.04		RS3	22
	64	2.56	2	0.08	SR2	RS4	26
	256	10.24	2	0.08		RS5	26
System B	2048	81.92	64	2.56	SR3	RS6	32
	8192	327.68	64	2.56		RS7	32
	32768	1310.72	2048	81.92	SR4	RS8	36
	131072	5242.88	2048	81.92		RS9	36
	524288	20971.52	32768	1310.72	SR5	RS10	40
	2097152	83886.08	32768	1310.72		RS11	40

Another scheme of resource sharing is employed for reaching higher integration time with relatively small in length shift registers that makes use of the already calculated sums. In the table is shown the configuration and the red coloured *RS* outputs representing their utilisation also as inputs for the adjacent shift registers.

Threshold and Masking Tables

For each detector's data, this system calculates 11 *Running Sums*. Every *Running Sum*, after every new calculation, is compared with its corresponding *Threshold* value that depends on the beam energy at that moment. If found to be higher then the *Comparator* will initiate a dump request. All requests are being gathered into a masking block with the purpose of distinguishing between "*Maskable*" and "*Unmaskable*" channels.



The tables are stored on the *BLM Mezzanine's* non-volatile memory and can be unique for each detector.

All outputs will be then summed and collected by the "*Combiner Card*" which will forward them to the "*Beam Interlock System*".