Design Specifications for a Radiation Tolerant Beam Loss Measurement ASIC

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Abstract: A novel radiation-hardened current digitizer ASIC is in planning stage, aimed at the acquisition of the current signals from the ionization chambers employed in the Beam Loss Monitoring system at CERN. The purpose is to match and exceed the performance of the existing discrete component design, currently in operation in the Large Hadron Collider (LHC). The specifications include: a dynamic range of nine decades, defaulting to the 1pA-1mA range but adjustable by the user, ability to withstand a total integrated dose of 10kGy at least in 20 years of operation and user selectable integrating windows, as low as 500ns. Moreover, the integrated circuit should be able to digitize currents of both polarity with a minimum number of external components and without needing any configuration. The target technology is the IBM 130nm CMOS process. The specifications, the architecture choices and the reasons on which they are based upon are discussed in this paper.

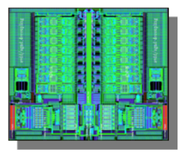
From the current discrete-component design...

FPGA VHDL Design

- Redundant data calculation for optical link and CRC32
- Triple redundancy with majority voting used in the most critical parts
- Hardwired clock used for critical parts
- Continuous function check
- I/O redundancy

12bit ADC

- CERN ASIC AD41240 from MIC group
- 4 channels, 40MS/s
- Radiation-tolerant design, up to 10 kGy
- Provides an increase in dynamic range
- And shorter response time

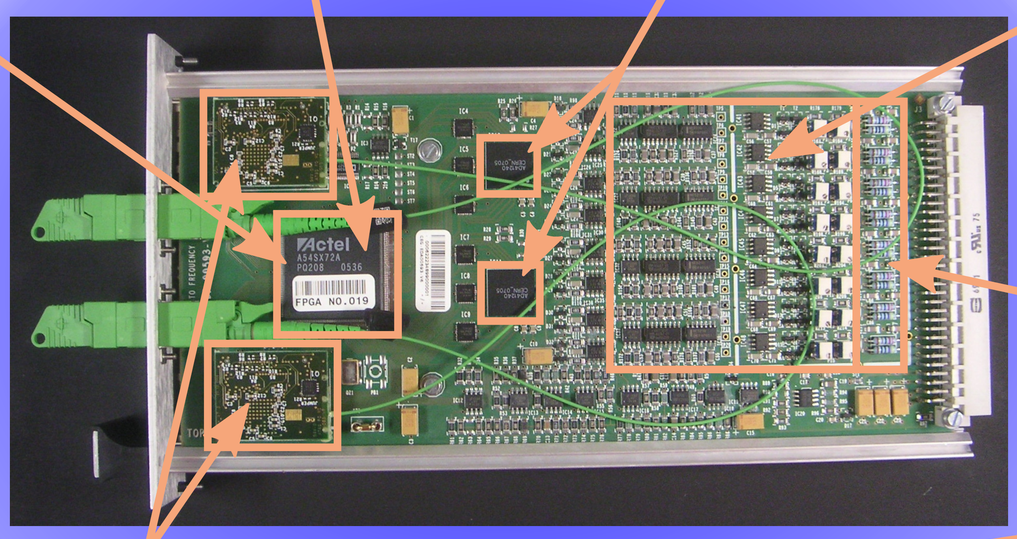


FPGA Hardware

- Actel anti-fuse FPGA A54SX32A
- 4024/2012 sequential and combinational cells
- No SEU detected up to $10^{-12} p/cm^2$
- Tested up to 480-790 Gy

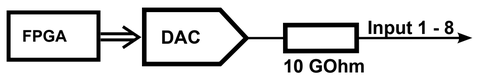
Charge balance integrator

- Reset injecting a fixed charge
- Independent of the characteristics of the integrator
- No blind time



Active offset compensation

- AD 5356 8 * 8 bit DAC
- Compensation of the offset current

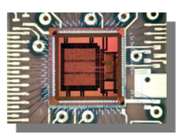


- Reset via HV distribution
- Tested up to 1.5 kGy

Input protection

- Over-voltage protection: 1.5 kV for 100us
- Leaded resistors for high power dissipation
- Special SMD capacitors with 1.5 kV break down voltage

Optical data link



- GOL Opto-Hybrid from CMS
- Gigabit optical link transmitter produced by CERN MIC
- Rad-tolerant design tested up to 2 kGy

Survey and test features

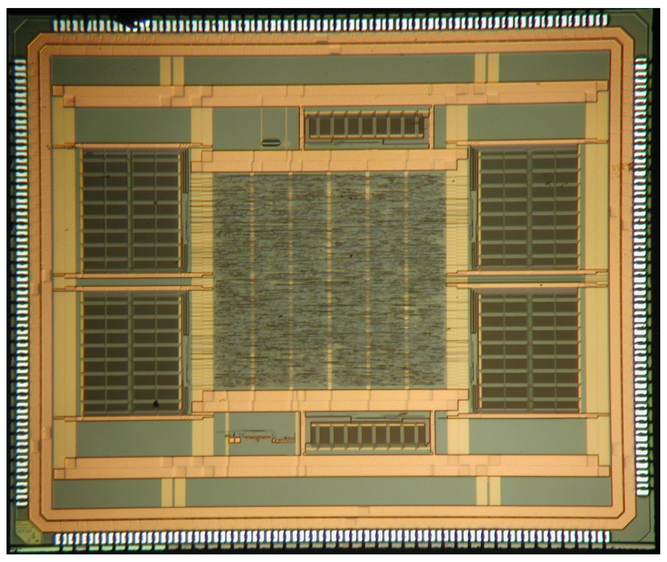
- Monitoring of the supply voltage
- Monitoring of the high voltage
- Monitoring of the input range
- Integrator level check

... to the new ASIC project.

Specifications for LHC upgrade

- Radiation-tolerant design up to 10kGy
- Dynamic range 1pA -1mA adjustable by the user
- Bipolar input current
- Integration window selectable by user, shortest time 500ns
- Direct interface with next generation gigabit optical link controller
- Compact and modular design

ASIC DESIGN



Solution

- Integration of the design in an ASIC
- Joint venture with MIC group at CERN
- Use of techniques of proven reliability from ASICs designed for the experiments

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