DESIGN SPECIFICATIONS FOR A RADIATION TOLERANT BEAM LOSS MEASUREMENT ASIC

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Abstract

A novel radiation-hardened current digitizer ASIC is in planning stage, aimed at the acquisition of the current signals from the ionization chambers employed in the Beam Loss Monitoring system at CERN. The purpose is to match and exceed the performance of the existing discrete component design, currently in operation in the Large Hadron Collider (LHC). The specifications include: a dynamic range of nine decades, defaulting to the 1 pA-1 mA range but adjustable by the user, ability to withstand a total integrated dose of 10 kGy at least in 20 years of operation and user selectable integrating windows, as low as 500 ns. Moreover, the integrated circuit should be able to digitize currents of both polarity with a minimum number of external components and without needing any configuration. The target technology is the IBM 130 nm CMOS process. The specifications, the architecture choices and the reasons on which they are based upon are discussed in this paper.

INTRODUCTION

It is expected that with the increase in LHC beam intensity an increase in beam losses will be observed as well. Accordingly, the BLM electronics installed in the facility will be exposed to a higher radiation level. The current discrete component front-end electronics will be replaced by an Application Specific Integrated Circuit (ASIC) chip, designed to operate in the radioactive environment and, at the same time, to deliver higher performance. The employment of the new integrated circuit will allow the placement of the acquisition boards closer to the detectors in the most radioactive locations.

DESIGN SPECIFICATIONS

The charge digitizer provides a digital output proportional to the integral of the input current over a time window. Figure 1 shows a functional diagram of the device.

The main objectives of the design are summarized as follows (Table 1):

- *Dynamic range*: nine decades (or 180 dB).
- *Minimum input current*: the ASIC design will be compatible with the different detectors and setups employed in the BLM system, in line with the specifications. Considering a current digitizer based on a current-to-frequency converter, the input-output relationship is given by $f_{OUT} = I_{in}/Q_{REF}$, where Q_{REF} is here referred to as the reference charge. Enabling the user to select different values of the reference charge provides an effective method to scale the maximum and minimum signals, while internally the range of frequencies of operation and the value of the DR are kept constant. As other design-dependent constraints affect the value of the maximum and minimum input currents, care should be taken in the implementation of different input ranges. Additionally, independently of the chosen design, the inverse saturation current of the protection diodes and its variation due to temperature, radiation effects and aging set a limit on the minimum detectable current that can be measured. To overcome this drawback, the protection circuit on the analog input pins will be opportunely designed, to decrease the lower limit under 1 pA. The trade-off between the overload tolerance of the custom-protected inputs and the input leakage will be analyzed to provide a satisfactory solution, to provide a leakage below 100 fA.
- *Bipolar input currents*: the converter should work with currents of either polarity, without requiring any pre-configuration. It is currently under consideration whether or not the converter will provide the same range for each of them or a full and a reduced one. The measurement of dual polarity currents with a single supply device requires the input to be biased at approximately $V_{DD}/2$. The availability of this voltage on an output pin is useful when a circuit is connected to the input and it is thus provided to the user (REFOUT pin in Fig. 1).
- *Radiation tolerance*: the design aims for a Total Ionizing Dose (TID) equal or greater than 10 kGy over a 20 years period. The requirements regarding Transient Dose Effects, maximum Single Event Effects (SEE) rates are being investigated and will be split into maximum Single Event Upsets (SEU) and Single Event Latch-up (SEL) rates.

In addition to the main features listed above, *the acquisition time window* should be selected by the user from a set, by means of dedicated setup pins, the shortest interval being 500 ns. Additionally, care should be taken in the design to ensure a *minimum number of external components*. The components required to assemble an acquisition board are one or more ASICs, a crystal, power management ICs and a controller for data transmission – depending on the selected transmission medium – and a few minor elements, such as decoupling capacitors . A diagram of an acquisition board is shown in Fig. 2, displaying the substantially reduced component count with respect to previous designs.

Table 1: Specifications of the LHC CFC Electronics [1] and ASIC

	Parameter	Value	Units	Comments
Current design	Dynamic range (DR)	nine decades		(1 pA-1 mA)
	Minimum detected current	1	pA	
	Linearity error	less than ±25	%	over the 1 nA-1 mA range
		less than ±100	%	over the 1 pA-1 nA range
	Integration window	40	μs	
	Total integrated dose	500	Gy	in 20 years
ASIC	Dynamic range	nine decades		positive and negative currents
	Minimum detected current	0.1	pA	User selectable, minimum value.
	Linearity error	less than ±25	%	over the upper six decades
		less than ±100	%	over the lower three decades
	Integration window	100, 40 or 0.5	μs	
	Total integrated dose	1×10^4	Gy	in 20 years

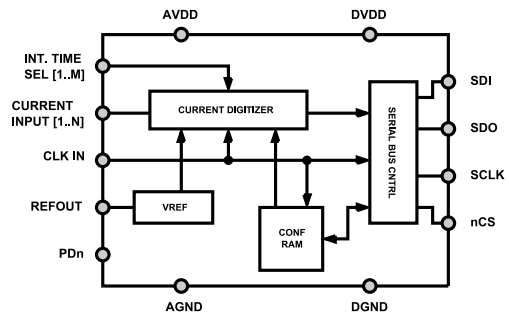

Figure 1: Functional diagram of the current digitizer.

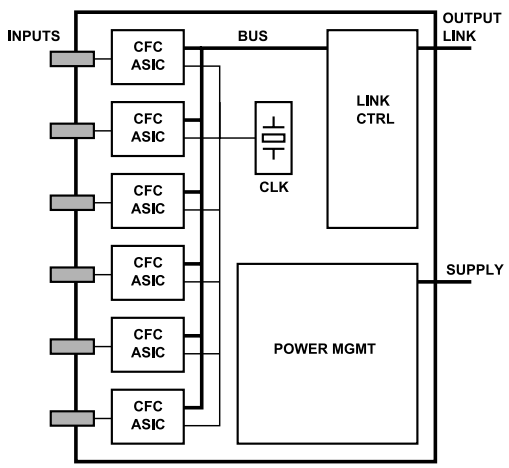

Figure 2: Diagram of an acquisition board showing the reduced number of components required (not to scale).

Several different *architectures* are being considered in the current preliminary study, including the use of a recycling integrator, multiple running integrators, a current steering multivibrator or a delta-sigma modulator. For each design, compatible schemes to provide a conversion within a user specified time window are being considered. A *digital output* shall be provided – therefore the ASIC is a current-input analog-to-digital converter (ADC). Depending on what type of device is to be used to read the output data and transmit it, a different type of bus or interface should be used, allowing a direct interface, which will provide a compatible data rate. As a dynamic range of nine decades requires 30bits, a serial bus allows a significant reduction in the number of output pins. In addition, a daisy chain wiring scheme would allow the connection of several devices on the same board while minimizing the number of wires, required in compact designs.

Although the operational *clock frequency* will be confirmed by system simulations, the design will be carried out for a relatively high clock rate, 10 MHz for the external clock and 100 MHz for the core one. The oscillator input will allow the direct connection of an external crystal.

Additional devices are considered to be included on the same chip: a *total dose sensor*, based on RADFETs. The knowledge of the radiation level to which each chip has been exposed to will give an estimate of the remaining life of the chip, and hence of when the board has to be serviced, and additionally it will provide useful information about the design and the technology itself for further developments. Moreover, since the analog-to-digital characteristic of the converter is affected by temperature changes, a *temperature sensor* will provide useful information to the surface electronics.

CONCLUSIONS

A radiation-tolerant ASIC will be developed at CERN to be employed in the foreseen LHC upgrade. The design will be carried out taking into account system-level specifications, the new devices that are concurrently developed, and will provide an increase in performance over the current design and additional functionality.

REFERENCES

[1] E Effinger, B Dehning, J Emery, G Ferioli, and C Zamantzas. Single gain radiation tolerant LHC beam loss acquisition card. (CERN-AB-2007-028), 2007.