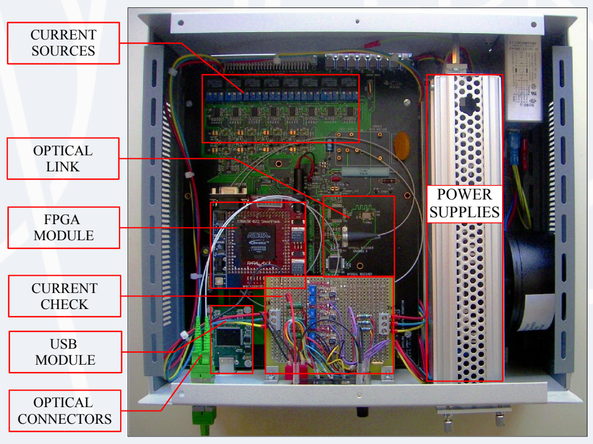
Functional and linearity test system for the LHC beam loss data acquisition card

J. Emery, B. Dehning, E. Effinger, C. Zamantzas, R. Leitner
CERN, Geneva, Switzerland

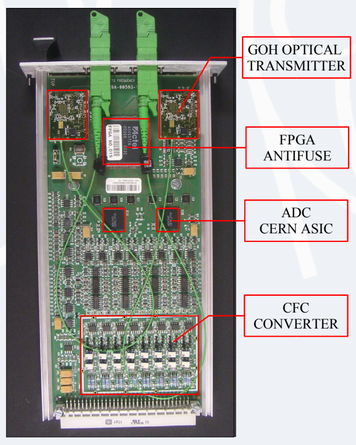
Abstract: In the frame of the design and development of the beam loss monitoring (BLM) system for the Large Hadron Collider (LHC) a flexible test system has been developed to qualify and verify during design and production the BLM LHC data acquisition card [1]. It permits to test completely the functionalities of the board as well as realizing analog input signal generation to the acquisition card. The system utilize two optical receivers, a Field Programmable Gate Array (FPGA), eights flexible current sources and a Universal Serial Bus (USB) to link it to a PC where a software written in LabWindows (National Instruments) runs. It includes an important part of the measurement processing [3] developed for the BLM in the future LHC accelerator [2]. The box is called Beam Loss Electronic Current to Frequency Tester (BLECFT).

System description

There will be around 650 acquisition cards to be calibrated and tested. Then they will be install inside the *LHC* tunnel. See [1]. The test box contain everything to test completely the tunnel card including a control unit (*FPGA* module) a power supply with current consumption check, two optical link to visualize the state of the tested broad and acquire data, eight current sources working in parallel to control the linearity of the measurement chain and an interface to the *PC* (*USB* module).



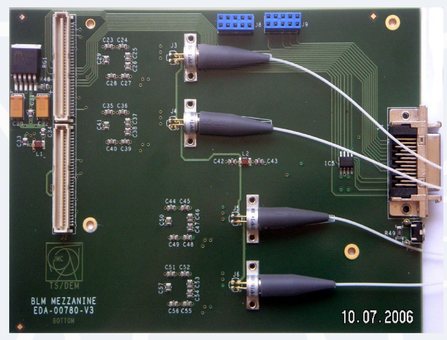
TEST SYSTEM BLECFT

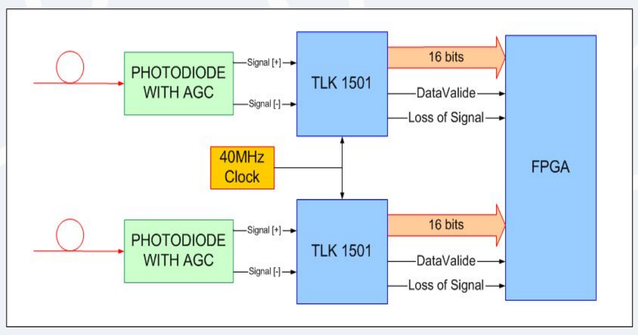


LHC ACQUISITION CARD

Optical link

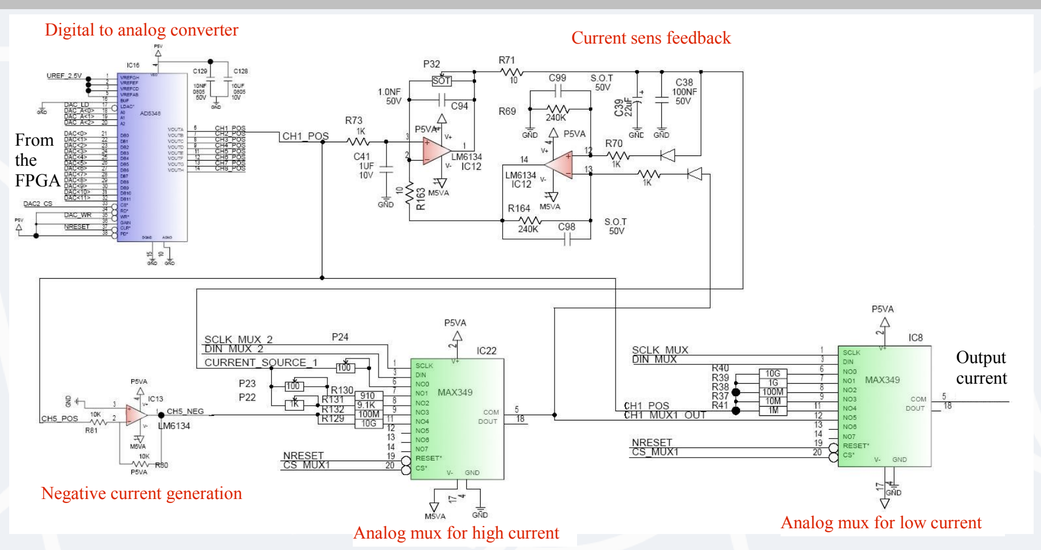
The data from the *BLM* acquisition card are send through an 800Mbps single mode optical link. The components have been taken from the receiver board of the *LHC* system (see right picture). The photodiode and the transceiver *(TLK 1501)* have been directly integrated on the board next to the *FPGA*. The data are demodulated by the *TLK* and send through the parallel bus @ 40MHz.





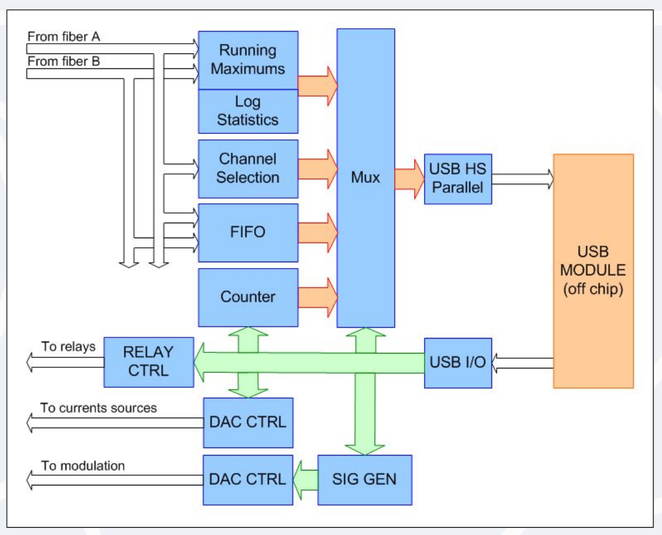
The tunnel card is sending every 40µs 20 words containing the identification number, the status of the card, the measurements of the *ADC* and the counter of the current to frequency circuit. These data are then processed inside the *FPGA* or send directly to the *PC*.

Current source



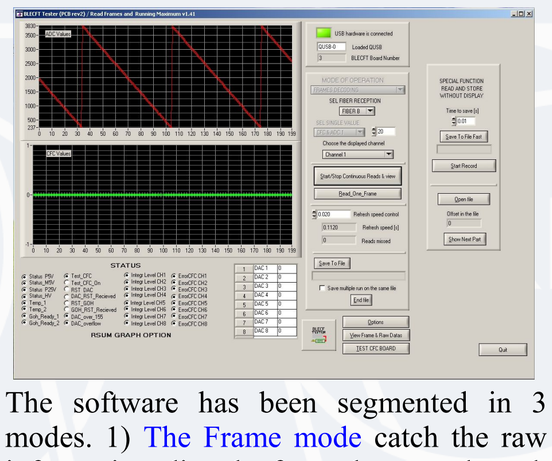
The current source provide current from 10pA to 1mA on eight channels in parallel. To calibrate it, the voltage reference can be changed with an Digital to analog converter (*DAC*). Since the input resistor of the board to be tested is 2.7 kOhm, the high current had to be designed separately from the rest with a current sens feedback. The low level currents uses high resistor values and the input resistance can be negligiate.

FPGA code



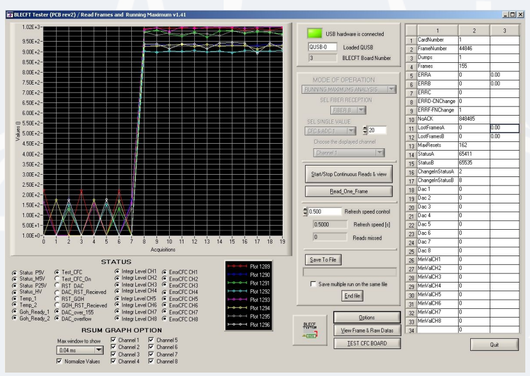
The type of FPGA used on the board is the same as the one of the *LHC BLM* system but smaller (Altera Stratix). The Running maximums permit to get similar data as the final *LHC* processing to realize test in real situations. To implement different modes, the description take advantage of the parallel processing of programmable logic to allow real time analysis of packets even during visualization in another mode. There are two data channels between the hardware and the computer. A slow speed for controlling the parameters of the tester and a high speed to download the data. There is also logic implemented to control the current sources through *DAC* converters, relays and analog switches.

Software



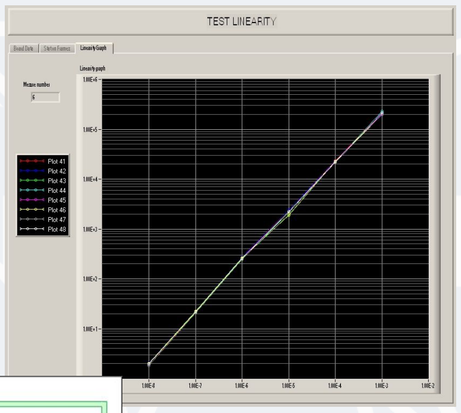
The software has been segmented in 3 modes. 1) The Frame mode catch the raw information directly from the tunnel card, analyze it and screen it as the data are. 2) The running maximum work exactly as the future *LHC* system [3]. The data are processed inside the *FPGA* and the software takes the results with a user defined period and show it.

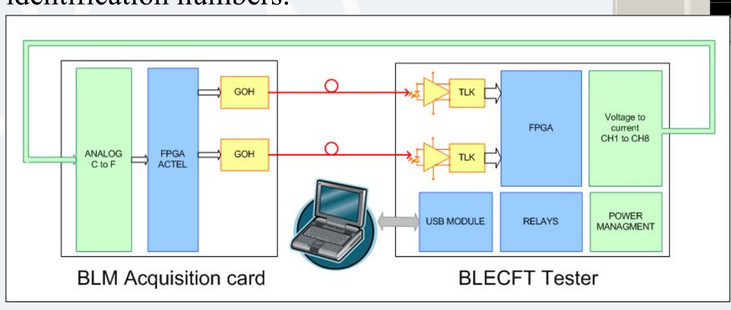
3) The oscilloscope mode permit to see all the data (40us period) of a given channel for a defined window. In mode 1 & 2, it is possible to visualize the status of the tested card, save the data shown on the screen and control the parameters like the current applied or the voltage which simulate the high voltage on the tunnel card.



Software test and calibration

There are numerous parameters to control during the functional test. The optical link connection (CRC check), the board status, the test mode response and the linearity of the inputs. In addition to the status informations survey, the system is used to calibrate accurately the gain and input offset current. A report is generated containing all the specific parameters of each tested boards including identification numbers.





In case of test failure, the severity is checked and reported in order to sort the boards and optimize the load of the repair team.

Complementary informations

[1] lecc06 ref. [49] The LHC beam loss monitoring system's data acquisition card by Ewald EFFINGER (CERN)
[2] lecc06 ref. [71] (Poster) The LHC Beam Loss Monitoring System's Surface Building Instalation by C. Zamantzas (CERN).
[3] "The Real-Time Data Analysis and Decision System for Particle Flux Detection in the LHC Accelerator at CERN.", Zamantzas, C., Brunel University, CERN-THESIS-2006-037.