# LHC Beam Loss Monitoring System

## LHC Beam Commissioning

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for the BLM team

# System overview
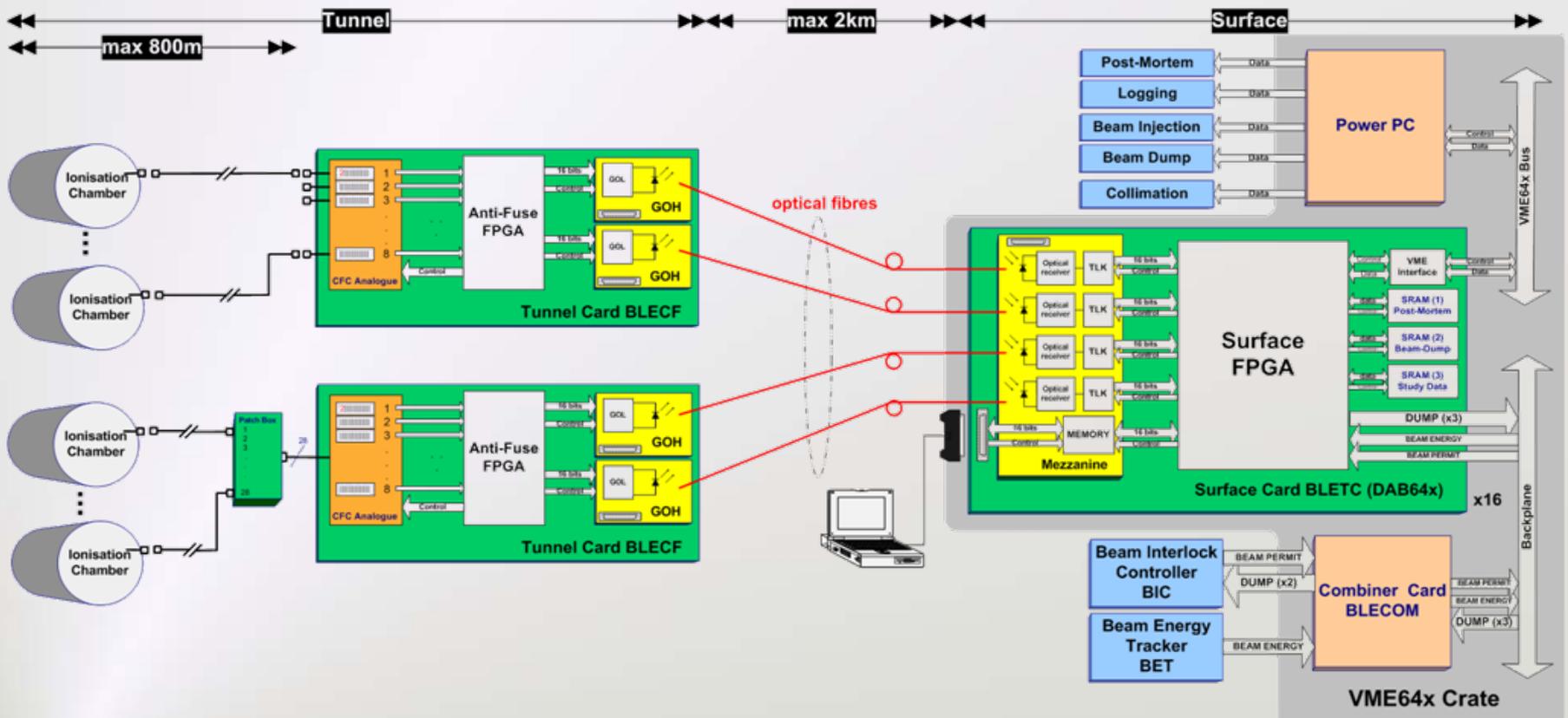
# Measurements

Examples of acquisition card's frequencies measured in the lab:

System Clock
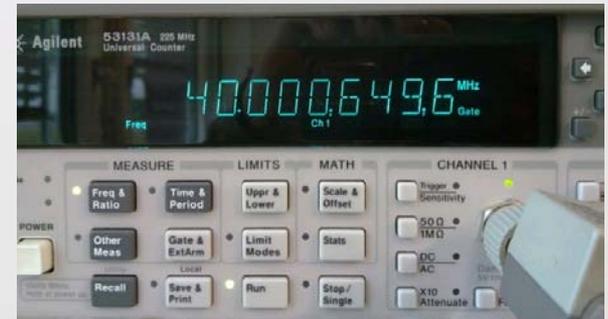




TX frequency





In short: Different data rates between cards received,
i.e more packets received if observesion over a long period (>1 sec).

# Solution

- Add the ability of writing 'half' packets
  - That is, when needed write data from only one BLECF and for symmetry the rest is filled with max values.

- Correction (clean-up) by front-end before dispatch
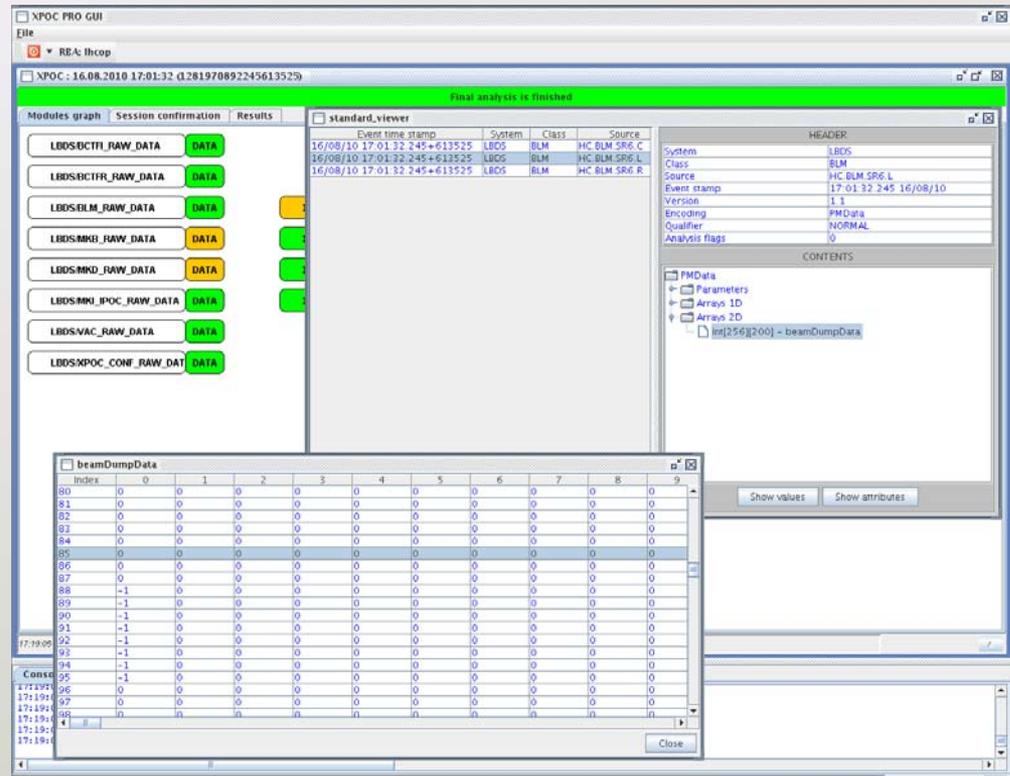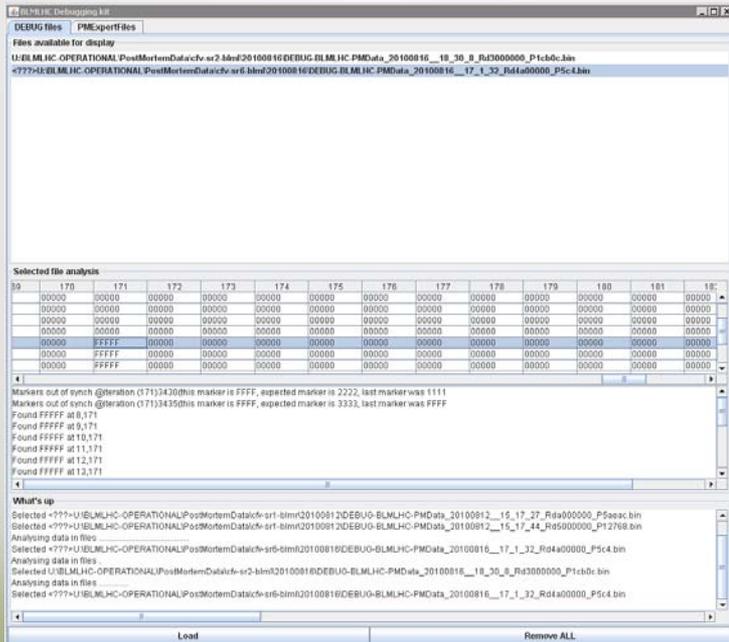
# System Verification Tests

A. Automatic extraction from DB + human inspection
   (repeated daily or weekly)

   - Frequency distribution of channel noise
   - Optical links degradation

   In the future will run inside the DB

B. Automatic on Vertical Slice Test system
   (before releasing new firmware)

   - Exhaustive Threshold triggering tests
   - Reception and Status tests
   - Linearity, impulse, and some predefined patterns of input signals check
   - [NEW] Inject predefined patterns in the XPOC and PM Buffers

# Test data in the PM/XPOC buffers

- Test firmware that replaces real values with data coming from incrementing counters.

- Automatic analysis of all Expert PM data

  - Checks continuity of values and the correct clean-up of 'half packets'.

  - (indirect check for LHC) checks that all SRAMs continue to function.
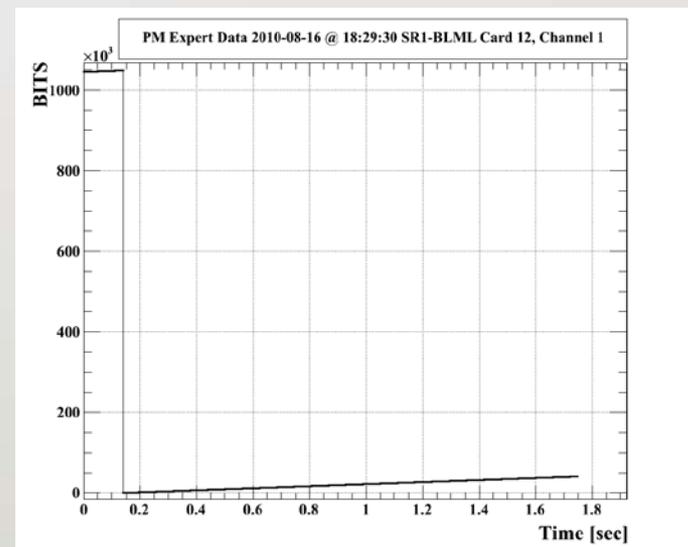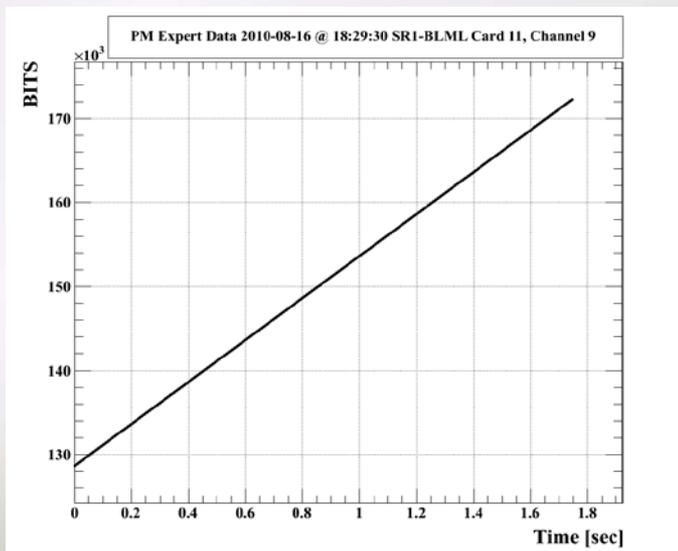
# Tests with pilot beams

Started at 03:20 tests with beam:

1. injected pilot beams, debunched them and dumped with the operator switch.

2. closed one of the collimator jaw of a TCP at point 3 and injected 3 times pilot beam 1.

# Debunched Beams

- all crates responded to GPM1

- all channels in SR6 have data and with the expected structure.

- expected difference between TCDSA channels of L and R is 40μs.
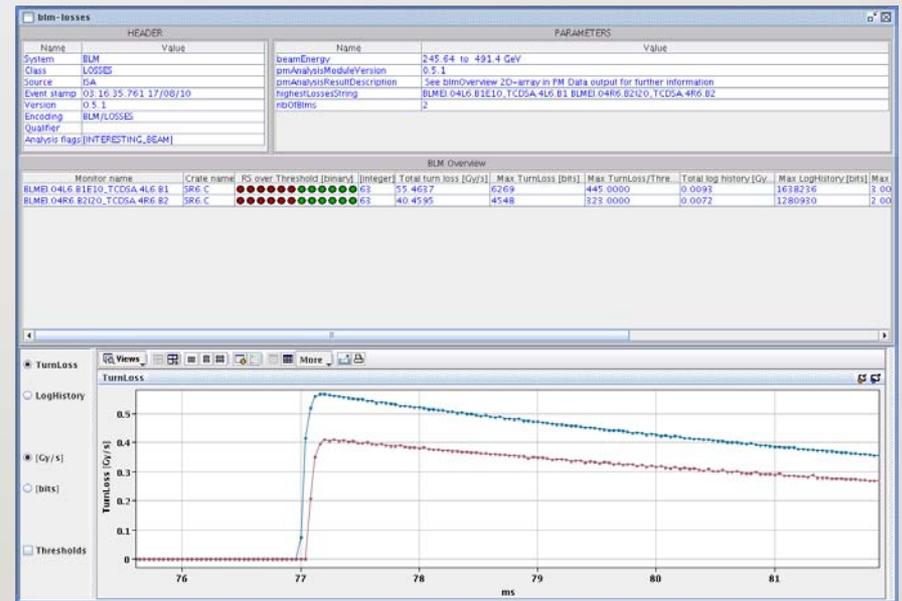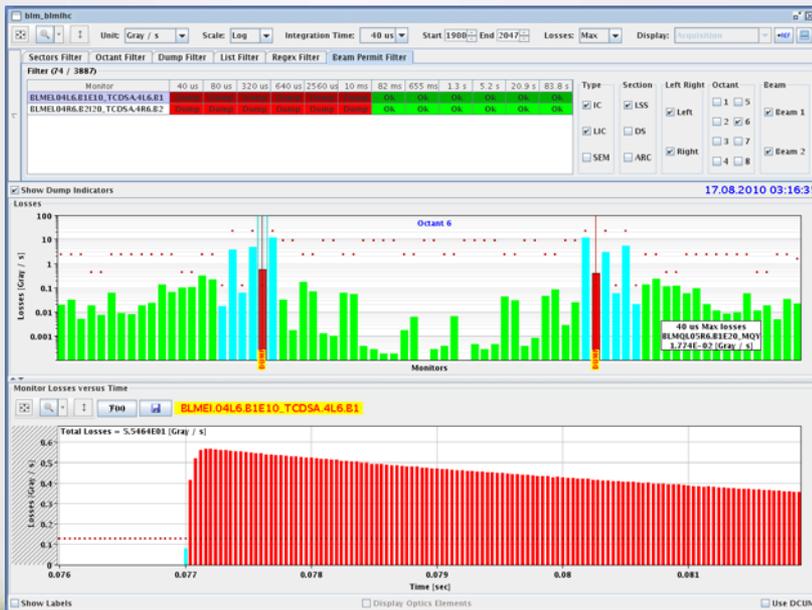
# Block Pilot Beam

- Closed collimator jaw at point 3
- Worst case scenario tested:
  - Thresholds at maximum (TCP)
  - Monitor/Electronic have to reach saturation
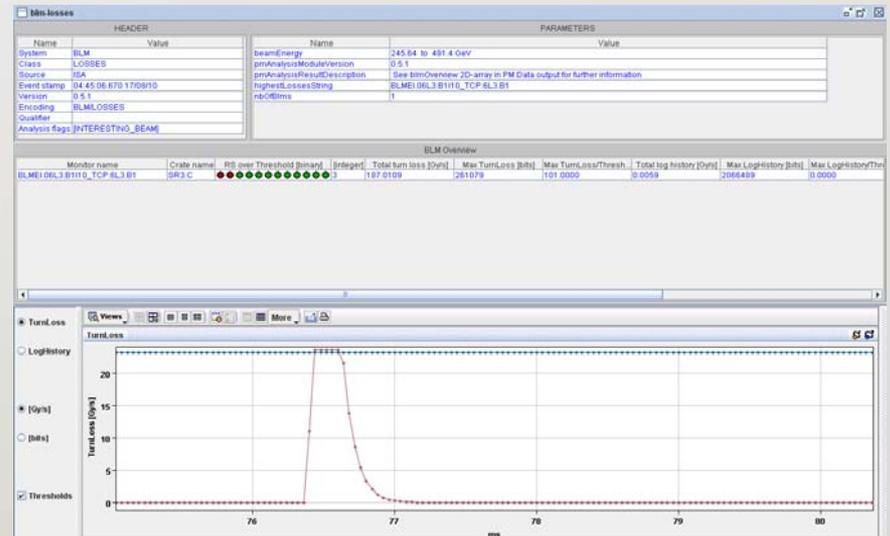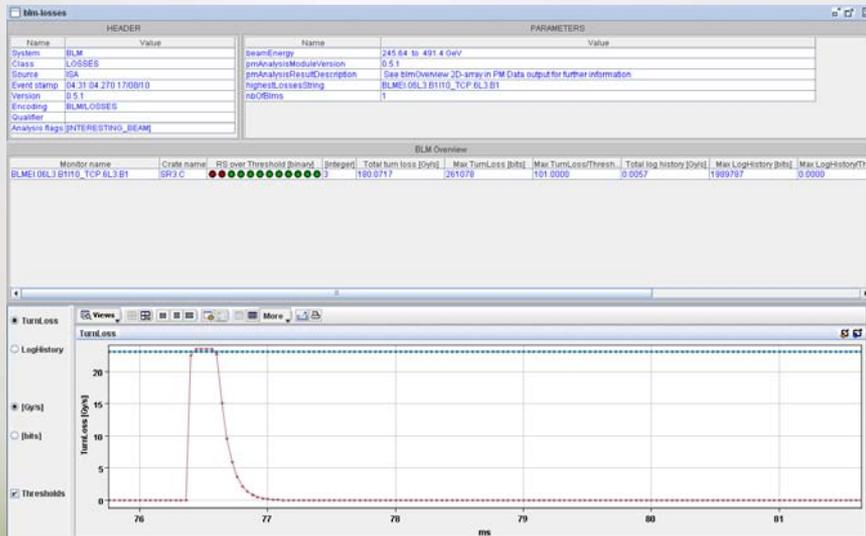
# System latency (2009 – 02/2010)

Analysed several Beam Dumps in detail.

Difference in time between the bunch at the MKI and the break of the beam permit loop (by the BLMS) recorded at the BIC was always between **100** and **130 μs**.

- Time of flight:
    - MKI => monitor = **10 μs**
    - monitor => acq. electronics (0.5 km cable) = **3 μs**
    - Acq. => processing electronics (1 km fibre) = **3 μs**
- Detection of change in frequency in the daisy-chain = **5 μs**
- Integration in the acquisition electronics = 40 μs.
- Decision at the BLETC (for fast losses) is taken every 40 μs.
- Processing of data to decide < 1 μs.

# System Latency (17/08/2010)

(MKI_timestamp + 80 μs) - BIC_timestamp

- 1282012264280683 + 80 - 1282012264280905 = 142 μs

- 1282013106680655 + 80 - 1282013106680861 = 126 μs

- **System latency < 90 μs**
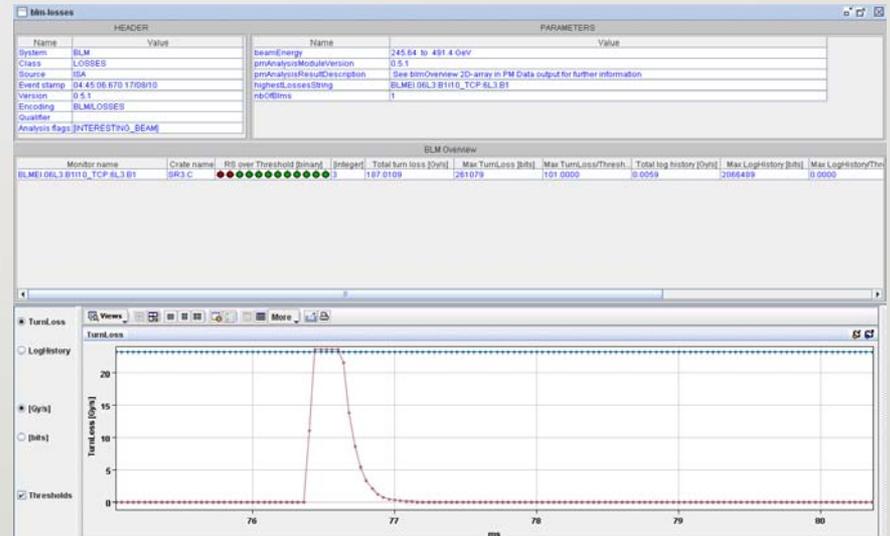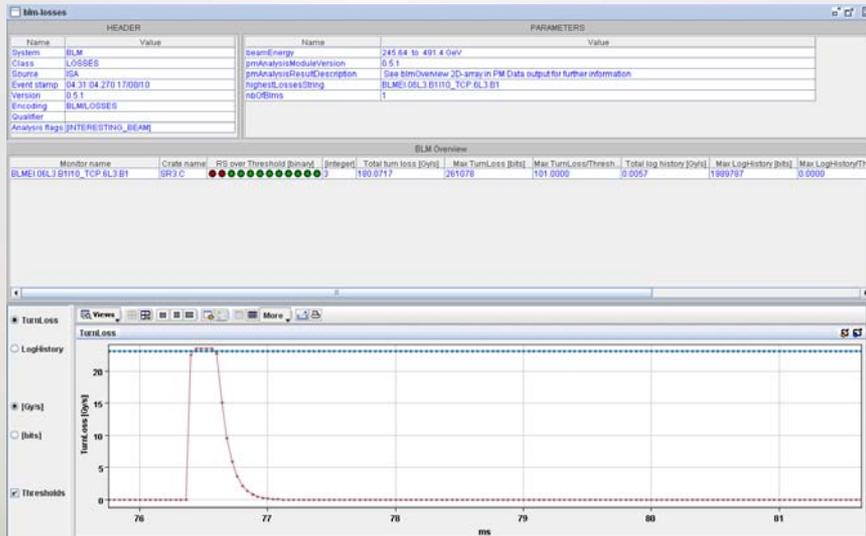
# Cooling

- **Added double fans in all racks**
  - Except SR1 and SR5 where only one fan
  - To be completed at next technical stop.

# Temperature of processing cards



CFV-SR2-BLMR:TEMPERATURE



CFV-SR7-BLML:TEMPERATURE
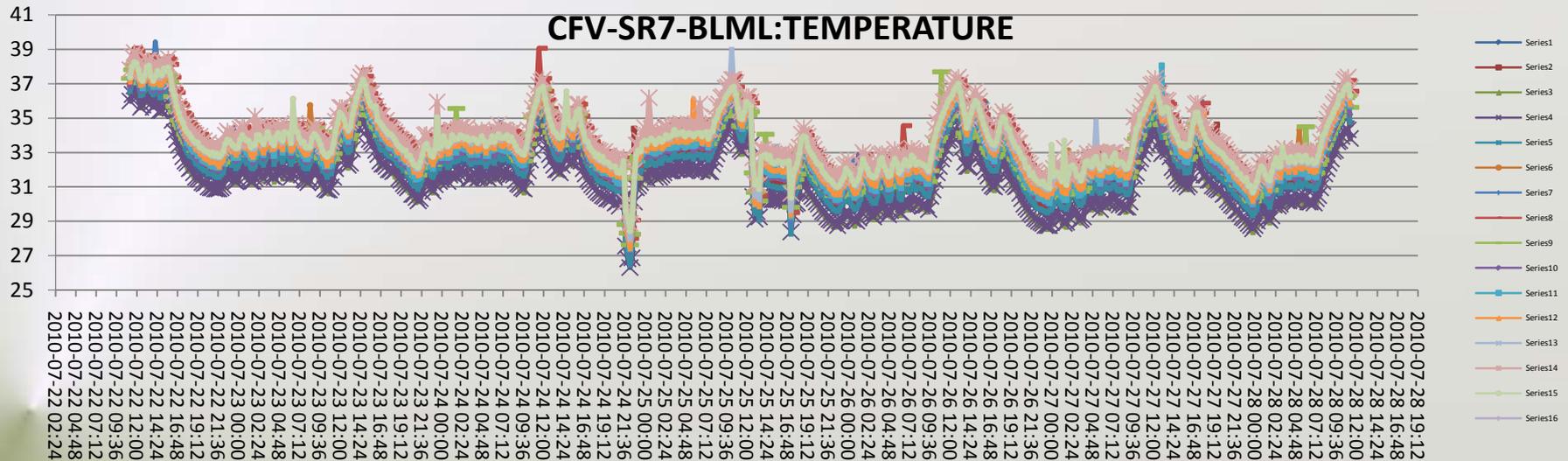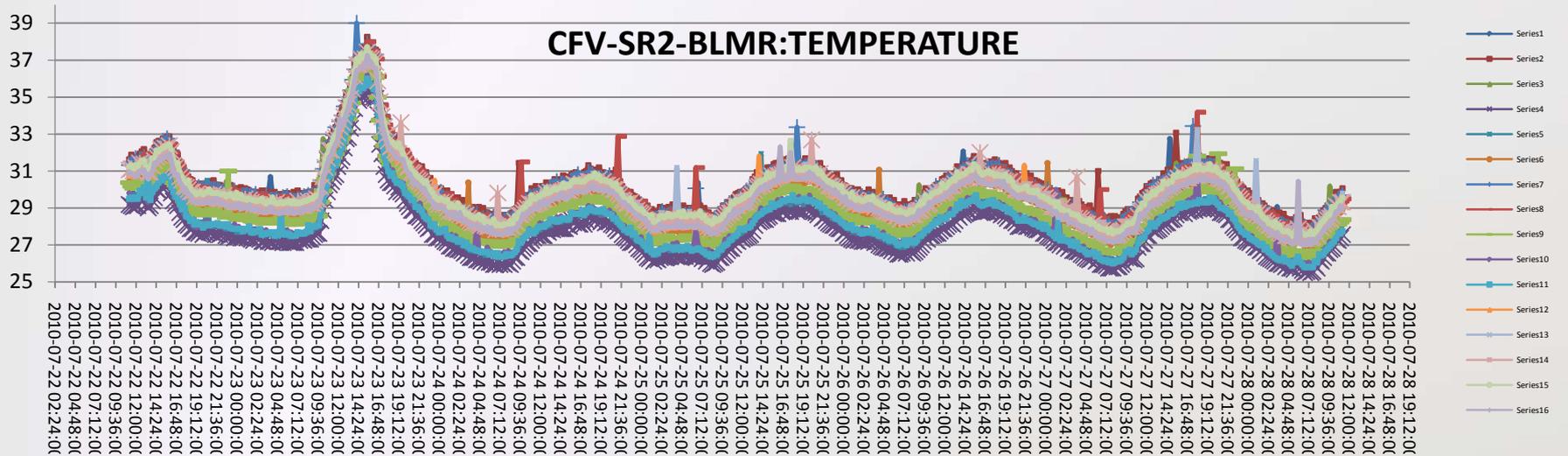
# CS-CCR-CMW4

- Too many 'critical' processes running on this machine
- Several of these processes show lag in sending data
- CO is following
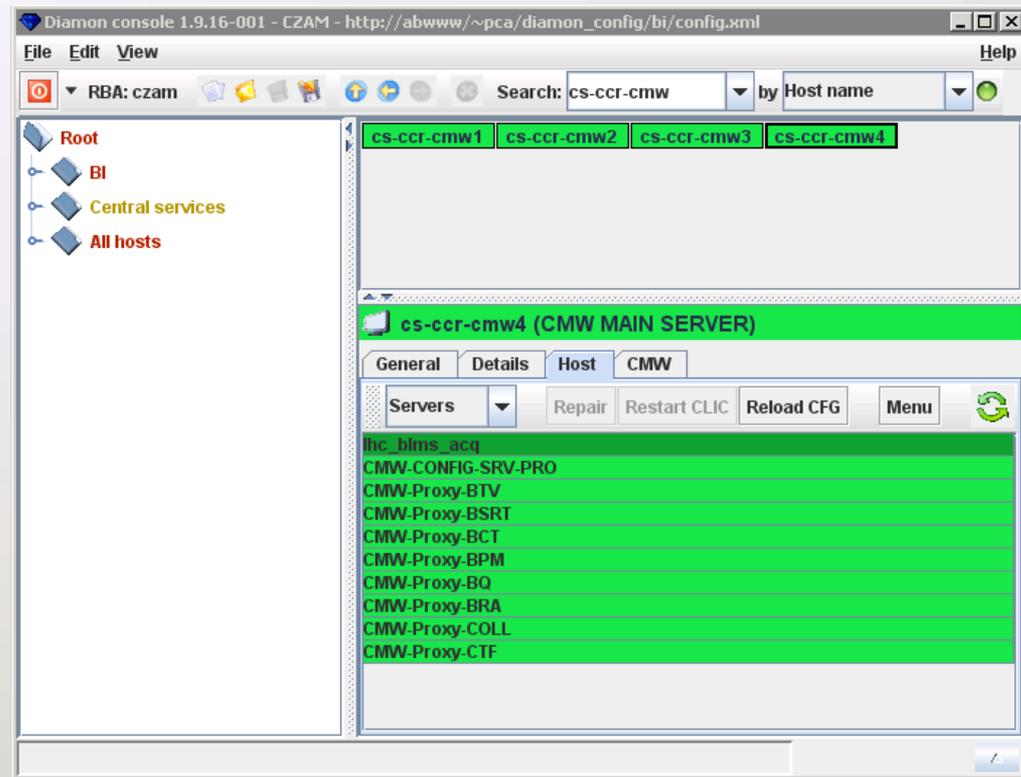
# Other

- Oscilloscope with PM triggering connected at point 7 to read the diamond detectors.

- Next technical stop will add a second oscilloscope with ACEMs.

Ewald Effinger

- SR7.R crate has not shown any issues since the intervention of 25/07
  - Was a series of broken CPUs.

Will be added back to SIS