Nov 6, 2000
TRIDAS
M.Dallavalle
INFN/Bologna

DT Track-Sorter-Master

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Since May:

- final prototype

- pASIC solution approved at the Muon Electronics System Review

- TSM irradiation tests: TID and SEE measurements

Choice of Technology

for developing the TSMS and TSMD ICs

- there is one TSM system per DT chamber
  a total of 250 TSMS and 500 TSMD ICs; a small production volume

- with FPGAs,
  - the same type of device can be used for both TSMS and TSMD
    (comparable number of pins in the chosen architecture)
    Flexibility in fine-tuning of the algorithms

  - sensitivity to the LHC radiation enviroment

A cost-effective solution is the “antifuse-FPGAs” also called pASICs (programmable ASICs)

Once programmed the chip configuration becomes permanent, making them effectively like ASICs

- tested for space applications pASICs have shown good tolerance to high radiation doses up to 10 to 50 krads and high thresholds for Single Event Effects

Compare to the radiation enviroment for the CMS Muon Barrel
(M.Huhtinen CMS COTS Workshop Nov.1999):

total neutron flux 3·10^10 1/cm^2 in 10 years
flux of>20 MeV n 1·10^9
Total Ionizing Dose 0.01 krad

- for a pASIC operating in the TSM of a DT chamber we expect
  no permanent damage and a negligible yearly SEU rate

The Actel A54SX is preferred

- slightly better performance and lower cost
- better CAD enviroment with VHDL entry for both design and simulation
- more accessible data on radiation tests and failure rates

Used chip logic resources:
69% TSMS
55% TSMD

- Enough margin for later developments

Actel A54SX32-3PQFP208
0.35 µm CMOS, 3.3 V
48,000 System Gates, 2880 Logic Modules, 1080 Register Cells
4.6 ns Clock-to-Out, 0.1 ns Input Set-up, 0.25 ns Clock Skew
Plastic Quad Flat Pack, 208 pins
Failure Rate 29.2 FITs (Actel reliability report 2000)
Mean Time Between Failures $3.43 \cdot 10^7$ hours
Power Consumption <200mW
Delivery time 6 months (temporary, due to large market demand)
Cost (extrapolat.) 76$/pc for 500 pcs

Irradiation tests

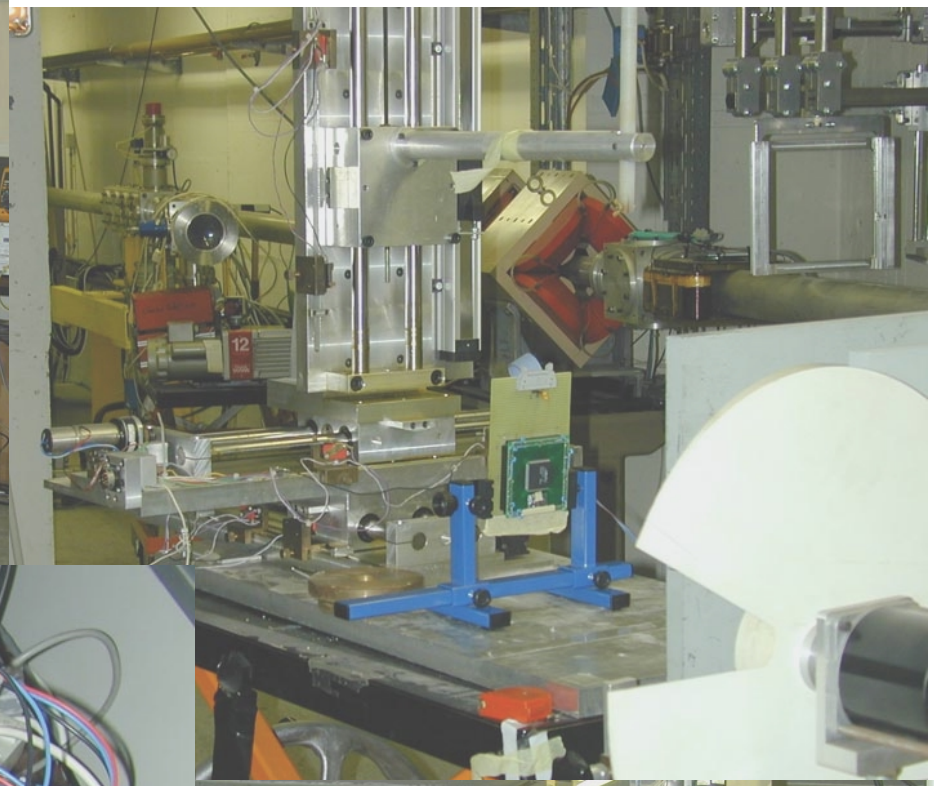
at the Cyclotron Research Centre (CRC) 59 Mev proton beam at the Universite Catholique de Louvain (UCL), Louvain-la-Neuve , Belgium

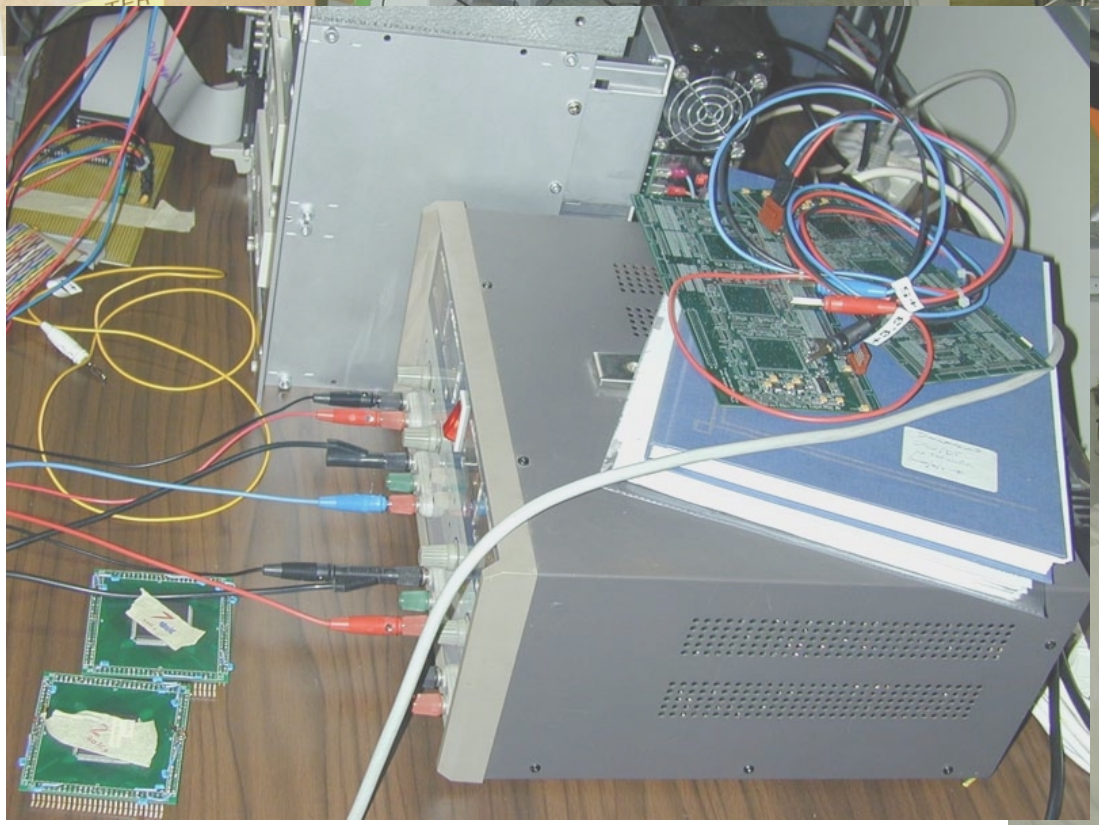
beam intensity 10^7 - 10^8 protons/cm2sec, 10 cm ∅
(10^10 protons/cm2 = 1.4 krads)

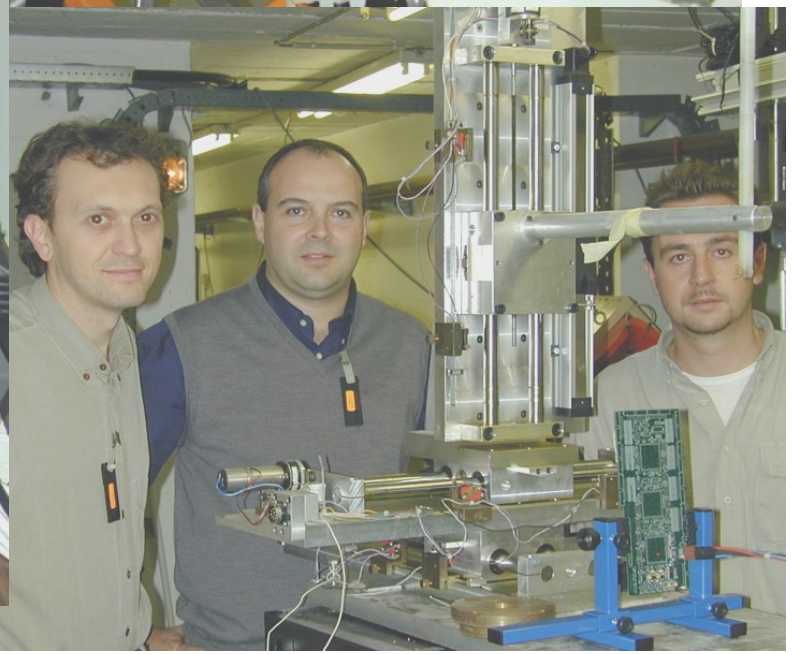
- Total Ionizing Dose tolerance
  - two TSM boards, instrumented with their passive components, drivers, bus switches,…, irradiated up to 0.5 krads/board
    - No failures, no significant increase in current

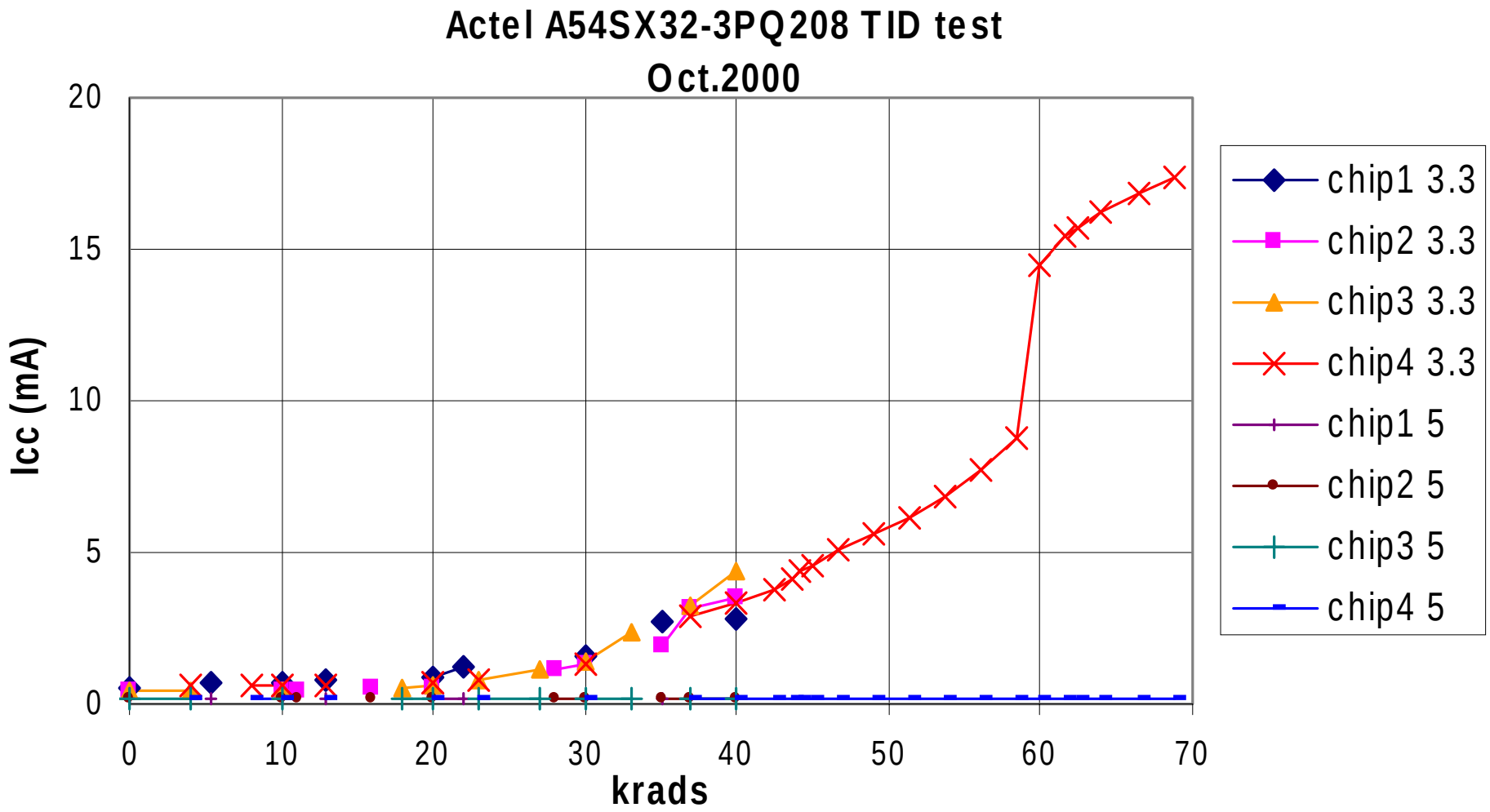
- Single Event Effects cross-section measurement
  - four pASICs, each implementing a 450 bit register, refreshed and monitored at 1 MHz, irradiated up to 40 krads/board (one of them up to 70 krads)
    - total fluence 1.4x10^12 protons/cm2
    - No latch-up, 1 transient upset event


PHILIPS








Actel A54SX32-3PQ208 TID test
Oct.2000
Icc (mA)
krads
0
5
10
15
20
0
10
20
30
40
50
60
70
chip1 3.3
chip2 3.3
chip3 3.3
chip4 3.3
chip1 5
chip2 5
chip3 5
chip4 5

Single Event Upset rate in CMS

- 1 observed event , then for the Actel A54SX32-3PQ208 chips tested

$\sigma_{SEU} <$ 2.9 /10^12 cm2 90% u.l. , for 59 MeV protons

- Following M.Huhtinen and F.Faccio (CMS COTS Workshop Nov. 1999) we calculate for the entire TSM system of 750 chips

$R <$ 2.2 SEU in 10 years of DT running