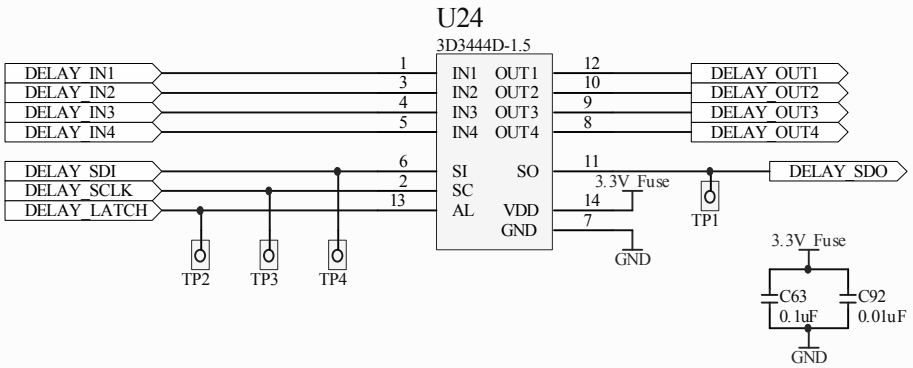

DAB64x: Delay Lines

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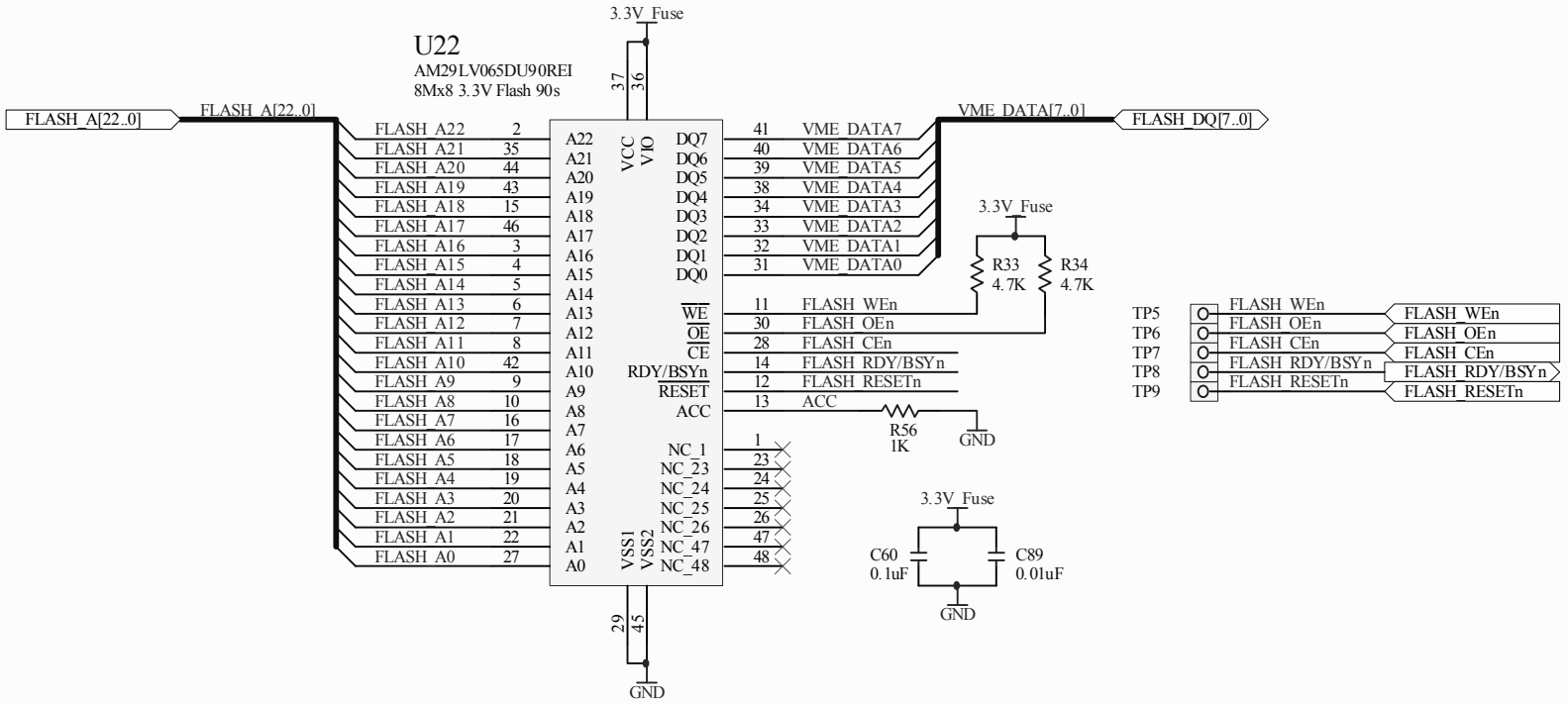

DAB64x: Flash Configuration Memory

Revision **0**	Drawing #:		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	Cannot open file G:\AHW\PROTEL\SCH_LIB\TRIUM
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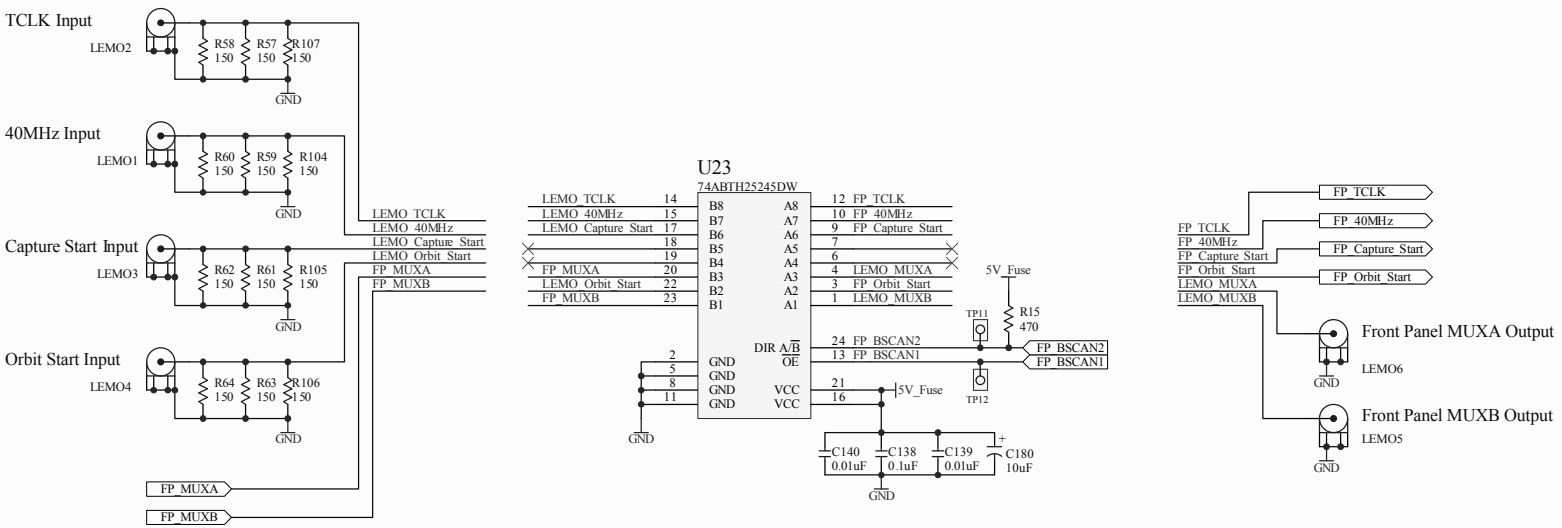
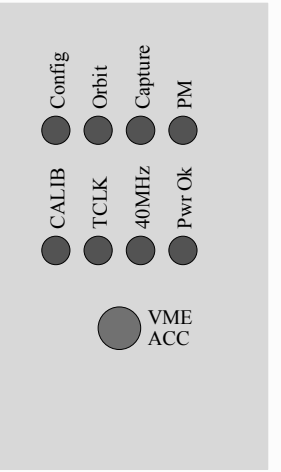
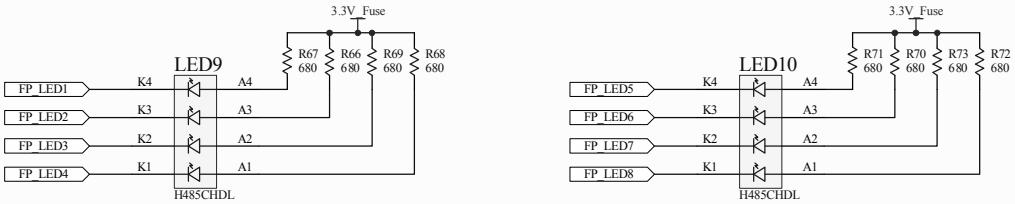
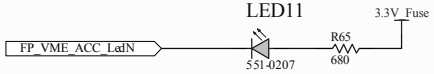


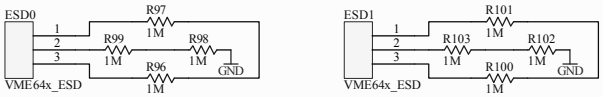






VME Access

ESD Front Panel Discharge Resistors



DAB64x: Front Panel Display and Signal I/O			
Revision **0**	Drawing #:	*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	Cannot open file G:\AHW\PROTEL\SCH_LIB\TRIU
	Sheet #: 4 of 13	Size: B	
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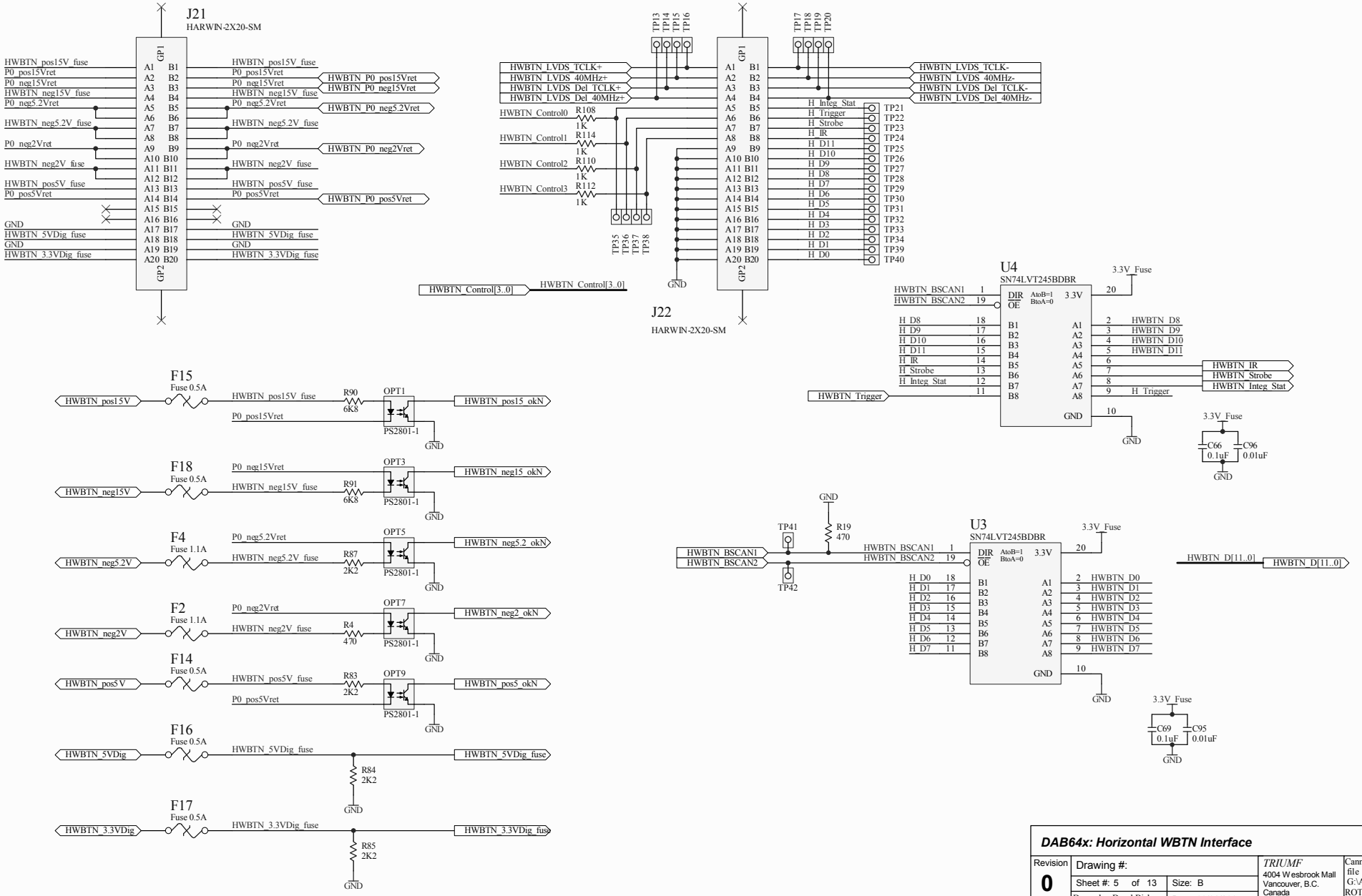
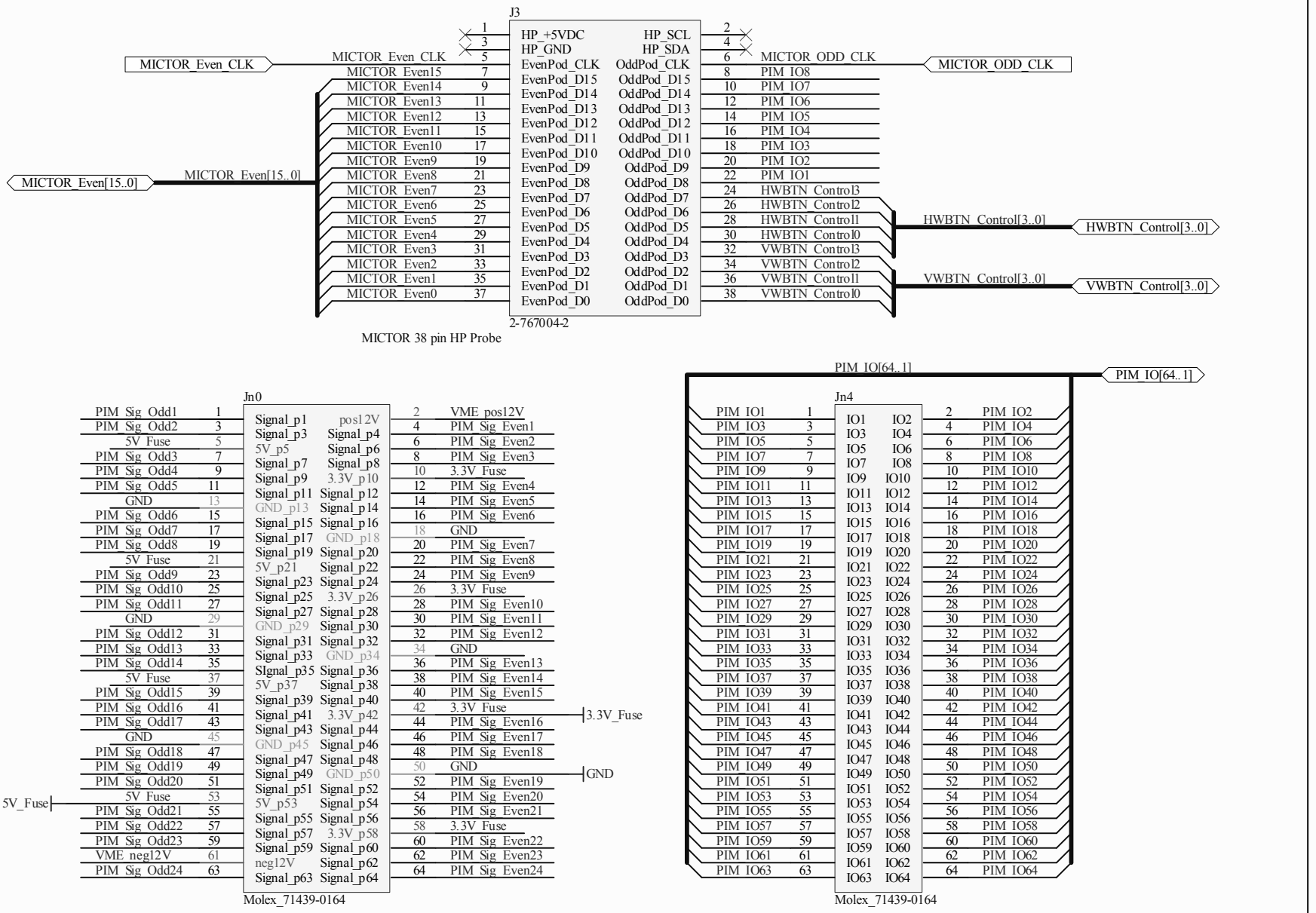
File: C:\AHW\CERN\DAB64x\Protel-DXP\DAB64x_FrontPanel.SchDoc			11:45:25


J21
HARWIN-2X20-SM
J22
HARWIN-2X20-SM
U4
SN74LVT245BDBR
U3
SN74LVT245BDBR
F15
Fuse 0.5A
F18
Fuse 0.5A
F4
Fuse 1.1A
F2
Fuse 1.1A
F14
Fuse 0.5A
F16
Fuse 0.5A
F17
Fuse 0.5A
PS2801-1
HWBTN_Control[3..0]
HWBTN_BSCAN1
HWBTN_BSCAN2
HWBTN_Trigger
HWBTN_D[11..0]
3.3V_Fuse
GND
DAB64x: Horizontal WBTN Interface
Revision
0
Drawing #:
Sheet #: 5 of 13
Size: B
Drawn by: Daryl Bishop
Date: 03/06/2004
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: C:\AHW\CERN\DAB64x\Protel-DXP\DAB64x_HWBTN.SchDoc



DAB64x: MICTOR Connector / PIM Mezzanine Connectors

Revision 0	Drawing #:		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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	Drawn by: TRIUMF	Date: 03/06/2004	
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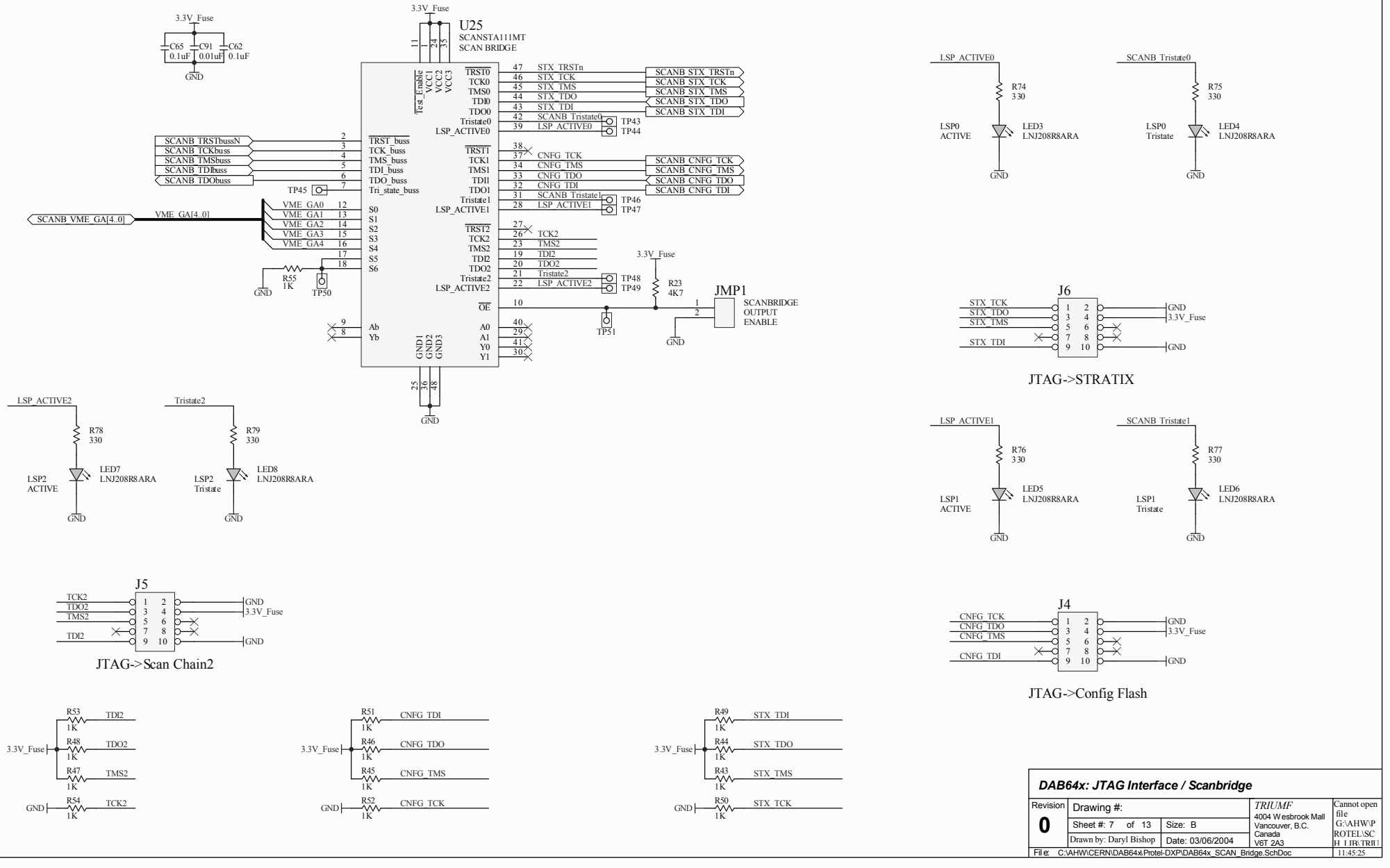

DAB64x: JTAG Interface / Scanbridge

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	Drawn by: Daryl Bishop	Date: 03/06/2004		
File: C:\AHW\CERN\DAB64x\Protel-DXP\DAB64x_SCAN_Bridge.SchDoc				11:45:25

U100A
EPM3256ATC144-10

VME_Add17	1	I/O LabA
VME_Add16	2	I/O LabA
GND	3	GNDIO
CNFG_TDI	4	TDI/io LabB
FP_VME_acc_ledN	5	I/O LabB
VME_A24_selectN	6	I/O LabB
40MHz-Osc_Enable	7	I/O LabB
Stratix_cnfg_Request	8	I/O LabB
Stratix_245_oeN	9	I/O LabB
VME_IRQ_Level0	10	I/O LabB
VME_IRQ_Level2	11	I/O LabB
VME_DATA15	12	I/O LabF
GND	13	GNDIO
VME_IRQ_Level1	14	I/O LabF
CNFG_DFLT1_Lo	15	I/O LabF
CNFG_DFLT3_Hi	16	I/O LabF
GND	17	GNDIO
CNFG_DFLT2_Lo	18	I/O LabF
VME_DATA14	19	I/O LabF
CNFG_TMS	20	TMS/io LabC
Irq_Vector_enable	21	I/O LabG
Stratix_dtackN	22	I/O LabG
Stratix_Config_Page1	23	I/O LabG
3.3V_Fuse	24	VCCIO
Stratix_Config_Page0	25	I/O LabG
GND	26	GNDIO
Stratix_SYSFAILn	27	I/O LabG
Stratix_nSTATUS	28	I/O LacC
Stratix_nCONFIG	29	I/O LabC
Stratix_DCLK	30	I/O LabC
VME_Add3	31	I/O LabC
VME_Add4	32	I/O LabC
GND	33	GNDIO
VME_DATA13	34	I/O LabC
VME_DATA12	35	I/O LabC
VME_DATA11	36	I/O LabC

U100B
EPM3256ATC144-10

VME_AM3	37	I/O LabD
VME_AM2	38	I/O LabD
VME_AM4	39	I/O LabD
VME_wrN	40	I/O LabD
VME_AM5	41	I/O LabD
VME_LwordN	42	I/O LabD
VME_Add23	43	I/O LabD
VME_ds1N	44	I/O LabD
VME_ds0N	45	I/O LabH
VME_Add22	46	I/O LabH
VME_Add21	47	I/O LabH
VME_Add20	48	I/O LabH
VME_Add19	49	I/O LabH
3.3V_Fuse	50	VCCIO
3.3V_Fuse	51	VCCINT
GND	52	GNDINT
VME_AM0	53	I/O LabH
VME_AM1	54	I/O LabH
VME_Add15	55	I/O LabL
VME_Add14	56	I/O LabL
GND	57	GNDINT
3.3V_Fuse	58	VCCINT
GND	59	GNDIO
VME_Add13	60	I/O LabL
VME_Add12	61	I/O LabL
VME_Add11	62	I/O LabL
VME_Add10	63	I/O LabL
GND	64	GNDIO
VME_Add9	65	I/O LabL
VME_Add18	66	I/O LabP
VME_Add8	67	I/O LabP
VME_Add7	68	I/O LabP
VME_Add6	69	I/O LabP
VME_Add5	70	I/O LabP
VME_DATA9	71	I/O LabP
VME_DATA8	72	I/O LabP

U100C
EPM3256ATC144-10

3.3V_Fuse	73	VCCIO
VME_Add2	74	I/O LabO
VME_DATA10	75	I/O LabO
3.3V_Fuse	76	VCCIO
GND	77	GNDIO
VME_Add1	78	I/O LabO
VME_IackN	79	I/O LabO
VME_IackinN	80	I/O LabO
VME_iack_outN	81	I/O LabO
VME_245_oeN	82	I/O LabK
VME_dtackN	83	I/O LabK
VME_SYSFAILn	84	I/O LabK
GND	85	GNDIO
VME_DTACK_EN	86	I/O LabK
Flash_A0	87	I/O LabK
Flash_ceN	88	I/O LabK
CNFG_TCK	89	TCK/io LabK
VME_GAP	90	I/O LabJ
Flash_oeN	91	I/O LabJ
VME_DATA0	92	I/O LabJ
VME_DATA1	93	I/O LabJ
GND	94	GNDIO
3.3V_Fuse	95	VCCIO
VME_DATA2	96	I/O LabJ
VME_DATA3	97	I/O LabJ
Flash_A21	98	I/O LabN
VME_DATA4	99	I/O LabN
VME_DATA5	100	I/O LabN
VME_DATA6	101	I/O LabN
VME_DATA7	102	I/O LabN
VME_GA4	103	I/O LabN
CNFG_TDO	104	TDO/io LabN
GND	105	GNDIO
Flash_A10	106	I/O LabM
Flash_A19	107	I/O LabM
VME_GA3	108	I/O LabM

U100D
EPM3256ATC144-10

Flash_A20	109	I/O LabM
Flash_A17	110	I/O LabM
Flash_A22	111	I/O LabM
Flash_A16	112	I/O LabM
Flash_A15	113	I/O LabM
GND	114	GNDIO
3.3V_Fuse	115	VCCIO
Flash_A14	116	I/O LabI
Flash_A13	117	I/O LabI
Flash_A12	118	I/O LabI
FLASH_RESETn	119	I/O LabI
VME_GA2	120	I/O LabI
VME_GA1	121	I/O LabI
VME_GA0	122	I/O LabI
3.3V_Fuse	123	VCCINT
GND	124	GNDINT
40MHZ_OSC2	125	GCLK1/INPUT
Stratix_CONFIG_DONE	126	OE1/INPUT
VME_sysresetN	127	GCLRn/INPUT
FLASH_RDY/BSYn	128	GCLK2/INPUT
GND	129	GNDINT
3.3V_Fuse	130	VCCINT
Flash_A11	131	I/O LabE
Flash_A9	132	I/O LabE
Flash_A8	133	I/O LabE
Flash_weN	134	I/O LabE
GND	135	GNDIO
Flash_A18	136	I/O LabE
Flash_A7	137	I/O LabE
Flash_A6	138	I/O LabE
Flash_A5	139	I/O LabA
Flash_A4	140	I/O LabA
Flash_A3	141	I/O LabA
Flash_A2	142	I/O LabA
Flash_A1	143	I/O LabA
3.3V_Fuse	144	VCCIO

TP52

3.3V_Fuse

C141 0.001uF C142 0.001uF C143 0.001uF C144 0.001uF C145 0.001uF C146 0.001uF C147 0.001uF C148 0.001uF C172 0.001uF

GND

3.3V_Fuse

C68 0.1uF C70 0.1uF C71 0.1uF C72 0.1uF C73 0.1uF C74 0.1uF C75 0.1uF C77 0.1uF C173 0.1uF

GND

VME Interface

CNFG_VME_Add[23..1]	VME_Add[23..1]
CNFG_VME_DATA[15..8]	VME_DATA[15..8]
CNFG_Flash/VME_Data[7..0]	VME_DATA[7..0]
CNFG_VME_AM[5..0]	VME_AM[5..0]
CNFG_VME_wrN	VME_wrN
CNFG_VME_LwordN	VME_lwordN
CNFG_VME_ds0N	VME_ds0N
CNFG_VME_ds1N	VME_ds1N
CNFG_VME_245oeN	VME_245_oeN
CNFG_VME_dtackN	VME_dtackN
CNFG_VME_DTACK_EN	VME_DTACK_EN
CNFG_VME_IRQ_Level[2..0]	VME_IRQ_Level[2..0]
CNFG_VME_iackN	VME_iackN
CNFG_VME_IackinN	VME_iackinN
CNFG_VME_iack_outN	VME_iack_outN
CNFG_VME_sysresetN	VME_sysresetN
CNFG_FP_VME_acc_ledN	FP_VME_acc_ledN
CNFG_VME_A24_selectN	VME_a24_selectN
CNFG_VME_GA[4..0]	VME_GA[4..0]
CNFG_VME_GAP	VME_GAP
CNFG_Stratix_cnfg_Request	Stratix_cnfg_Request
CNFG_Stratix_dtackN	Stratix_dtackN
CNFG_Stratix_245oeN	Stratix_245_oeN
CNFG_Irq_Vector_enable	Irq_Vector_enable
CNFG_VME_SYSFAILn	VME_SYSFAILn
CNFG_Stratix_SYSFAILn	Stratix_SYSFAILn
CNFG_Stratix_Config_Page[1..0]	Stratix_Config_Page[1..0]

JTAG/Boundary Scan

CNFG_TCK	CNFG_TCK
CNFG_TMS	CNFG_TMS
CNFG_TDI	CNFG_TDI
CNFG_TDO	CNFG_TDO
CNFG_DFLT2_Lo	CNFG_DFLT2_Lo
CNFG_DFLT1_Lo	CNFG_DFLT1_Lo
CNFG_DFLT3_HI	CNFG_DFLT3_Hi

Stratix Configuration

CNFG_40MHz-Osc_Enable	40MHZ-Osc_Enable
CNFG_40MHz-Clock	40MHZ_OSC2
CNFG_Stratix_DCLK	Stratix_DCLK
CNFG_Stratix_nCONFIG	Stratix_nCONFIG
CNFG_Stratix_nSTATUS	Stratix_nSTATUS
CNFG_Stratix_CONFIG_DONE	Stratix_CONFIG_DONE

Flash Memory

CNFG_Flash_A[22..0]	Flash_A[22..0]
CNFG_Flash_weN	Flash_weN
CNFG_Flash_ceN	Flash_ceN
CNFG_Flash_oeN	Flash_oeN
CNFG_FLASH_RDY/BSYn	FLASH_RDY/BSYn
CNFG_FLASH_RESETn	FLASH_RESETn

DAB64x: Stratix Configuration Controller

Revision 0	Drawing #:		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 13	Size: B	
	Drawn by: Daryl Bishop	Date: 03/06/2004	
File: C:\AHW\CERN\DAB64x\Protel-DXP\DAB64x_Stratix_Configurator.SCHDOC			11:45:25

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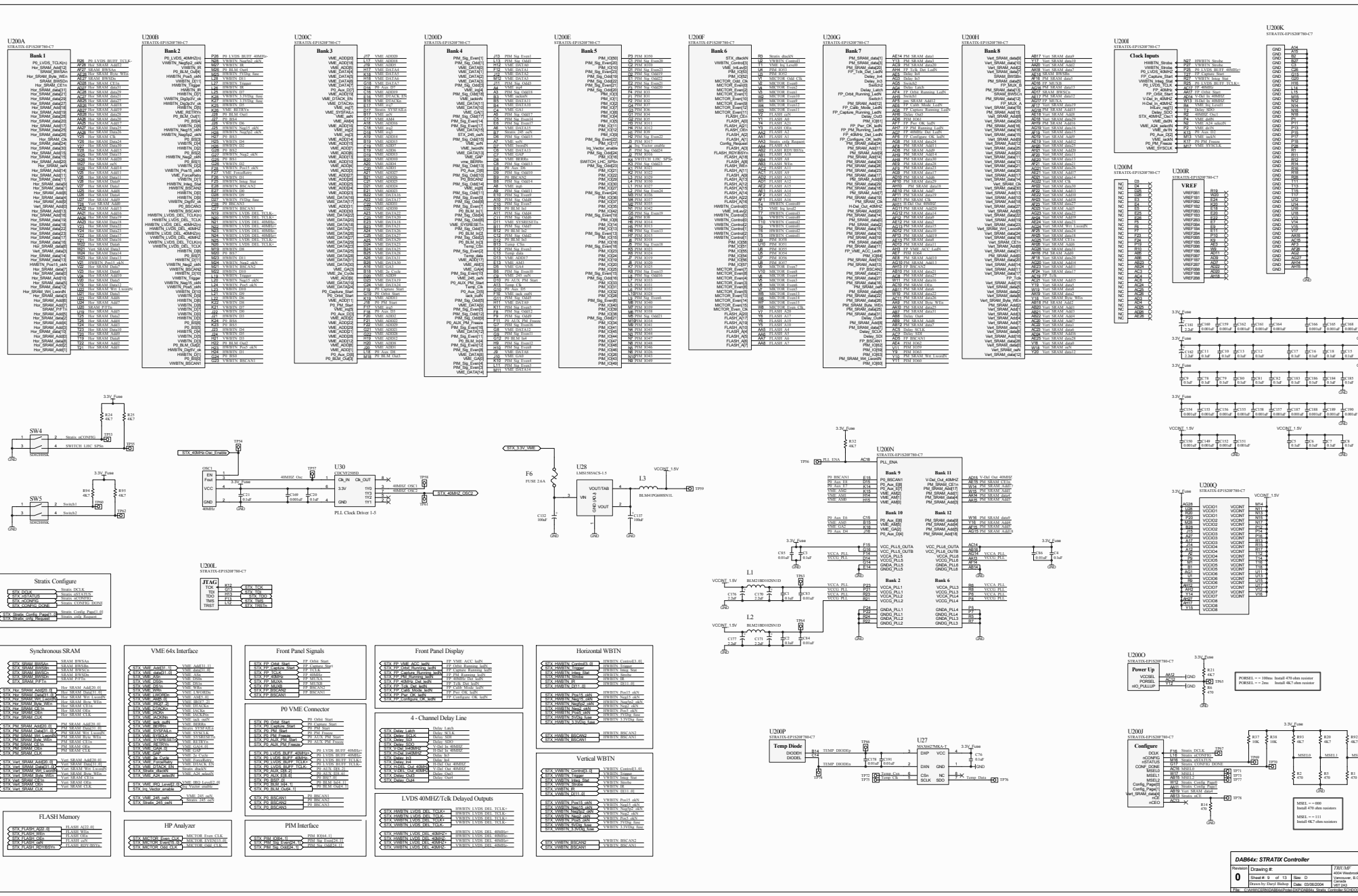
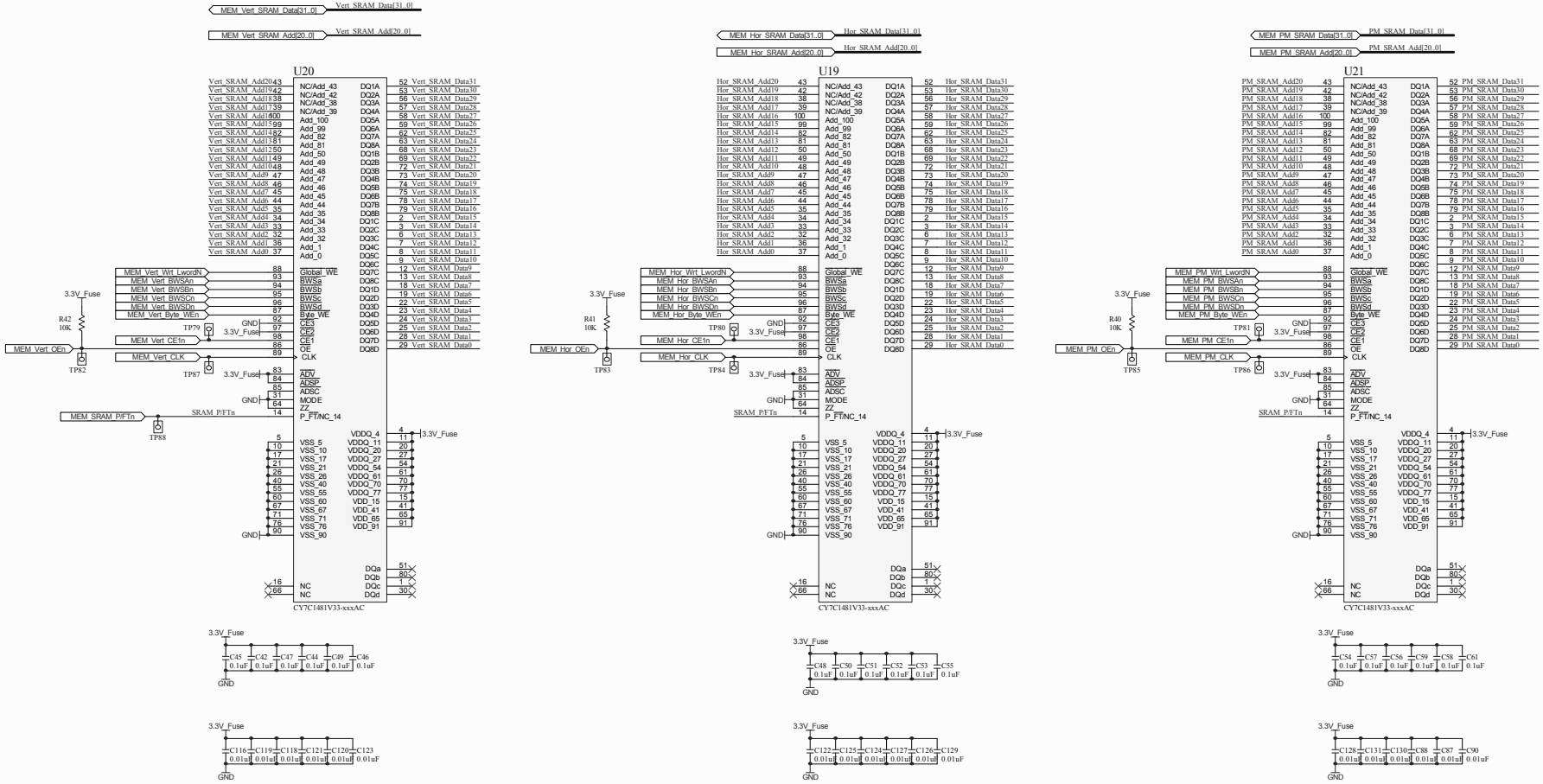

U200A
U200B
U200C
U200D
U200E
U200F
U200G
U200H
U200I
U200K
U200M
U200R
U200L
U200N
U200O
U200P
U200Q
U200J
SW4
SW5
U30
U28
L3
L1
L2
F6
Stratix Configure
Synchronous SRAM
VME 64x Interface
Front Panel Signals
Front Panel Display
Horizontal WBTN
P0 VME Connector
4 - Channel Delay Line
Vertical WBTN
LVDS 40MHZ/Telk Delayed Outputs
FLASH Memory
HP Analyzer
PIM Interface
DAB64x: STRATIX Controller



DAB64x: H,V & PM Synchronous SRAM

Revision	Drawing #:		
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	Drawn by: Daryl Bishop	Date: 03/06/2004	Cannot open file G:\AHW\PROTEL\SCH\

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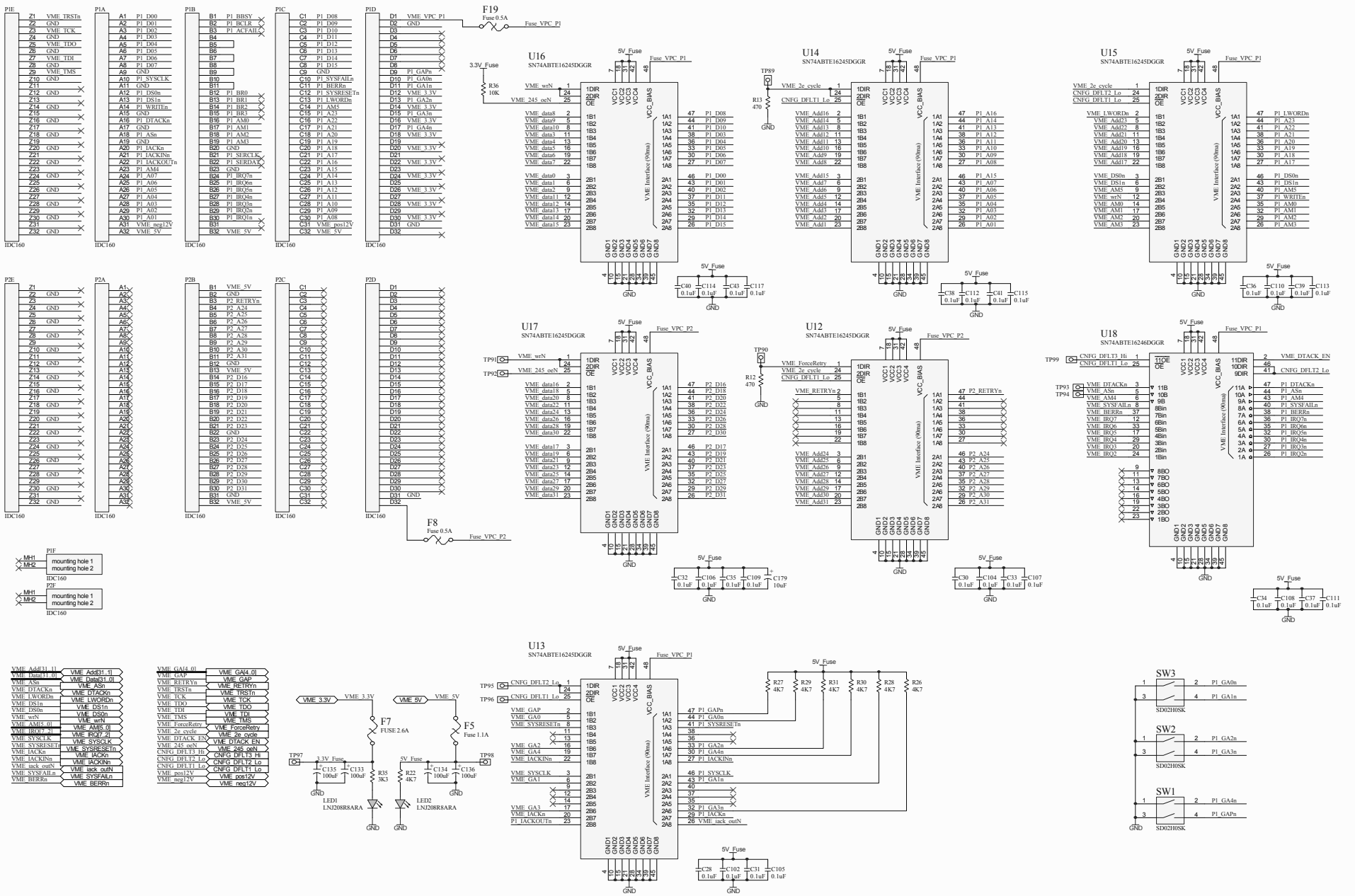
P1E
P1A
P1B
P1C
P1D
IDC160
F19
Fuse 0.5A
Fuse_VPC_P1
U16
U14
U15
SN74ABTE16245DGGR
5V_Fuse
3.3V_Fuse
R36
10K
TP89
R13
470
GND
P2E
P2A
P2B
P2C
P2D
F8
Fuse_VPC_P2
U17
U12
SN74ABTE16246DGGR
TP90
TP91
TP92
P1F
P2F
mounting hole 1
mounting hole 2
U13
TP95
TP96
F7
FUSE 2.6A
F5
Fuse 1.1A
TP97
TP98
LED1
LED2
LNJ208R8ARA
R27
R29
R31
R30
R28
R26
4K7
SW3
SW2
SW1
SD02H0SK
VME_Add[31..1]
VME_Data[31..0]
VME_GA[4..0]
VME_GAP
VME_RETRYn
VME_TRSTn
VME_TCK
VME_TDO
VME_TDI
VME_TMS
VME_2e_cycle
VME_DTACK_EN
VME_245_oeN
CNFG_DFLT3_Hi
CNFG_DFLT2_Lo
CNFG_DFLT1_Lo
VME_pos12V
VME_neg12V
VME_ASn
VME_DTACKn
VME_LWORDn
VME_DS1n
VME_DS0n
VME_wrN
VME_AM[5..0]
VME_IRQ[7..2]
VME_SYSCLK
VME_SYSRESETn
VME_IACKn
VME_IACKINn
VME_iack_outN
VME_SYSFAILn
VME_BERRn
DAB64x: VME Interface P1/P2 Connectors
Revision
0
Drawing #:
Sheet#: 11 of 13
Size: C
Drawn by: Daryl Bishop
Date: 03/06/2004
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4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
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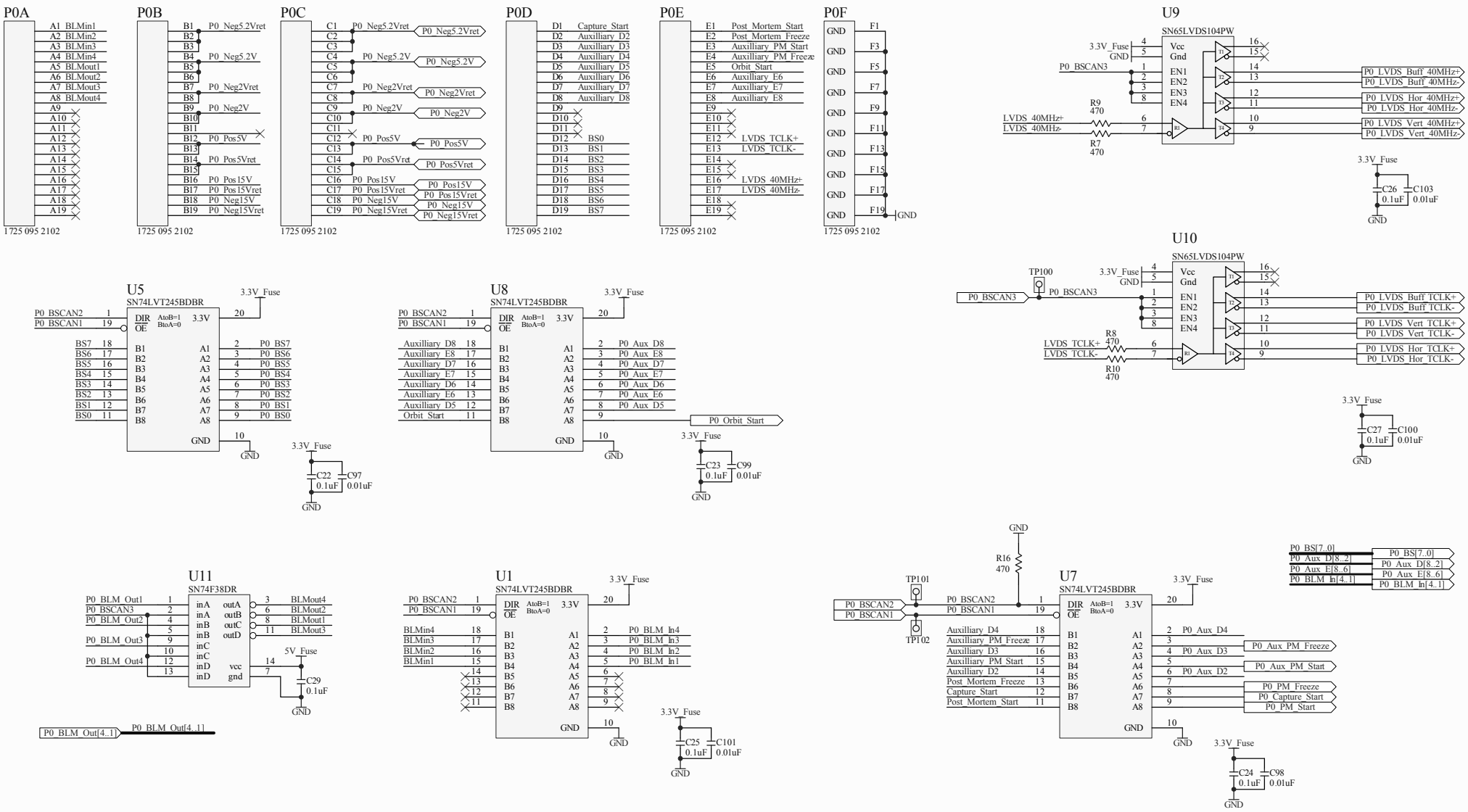

DAB64x: VME P0 Interface

Revision	Drawing #		TRIUMF	Cannot open file
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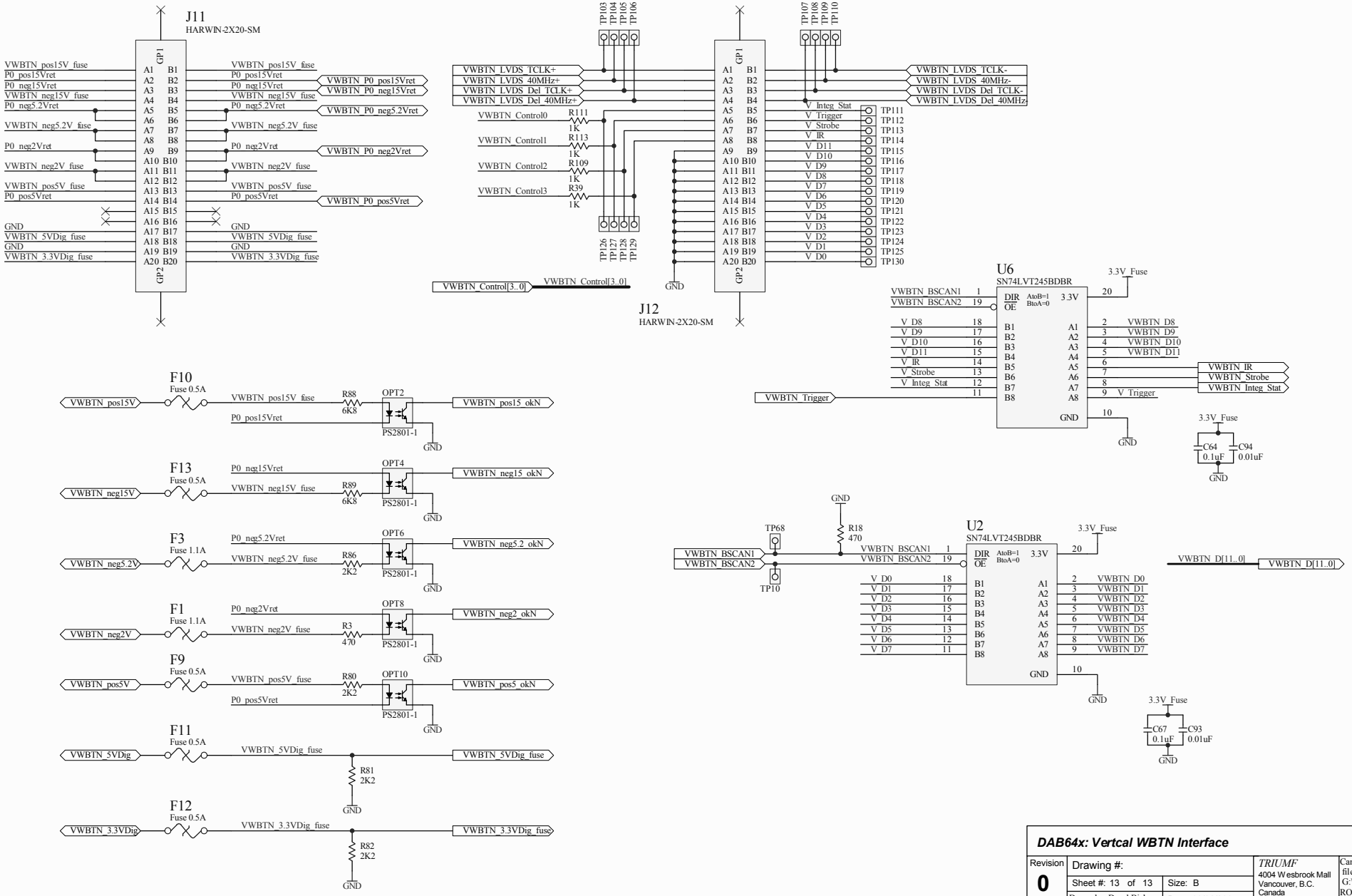

DAB64x: Vertcal WBTN Interface

Revision	Drawing #		TRIUMF	Cannot open file G:\AHW\PROTEL\SCH_LIB\TRIU
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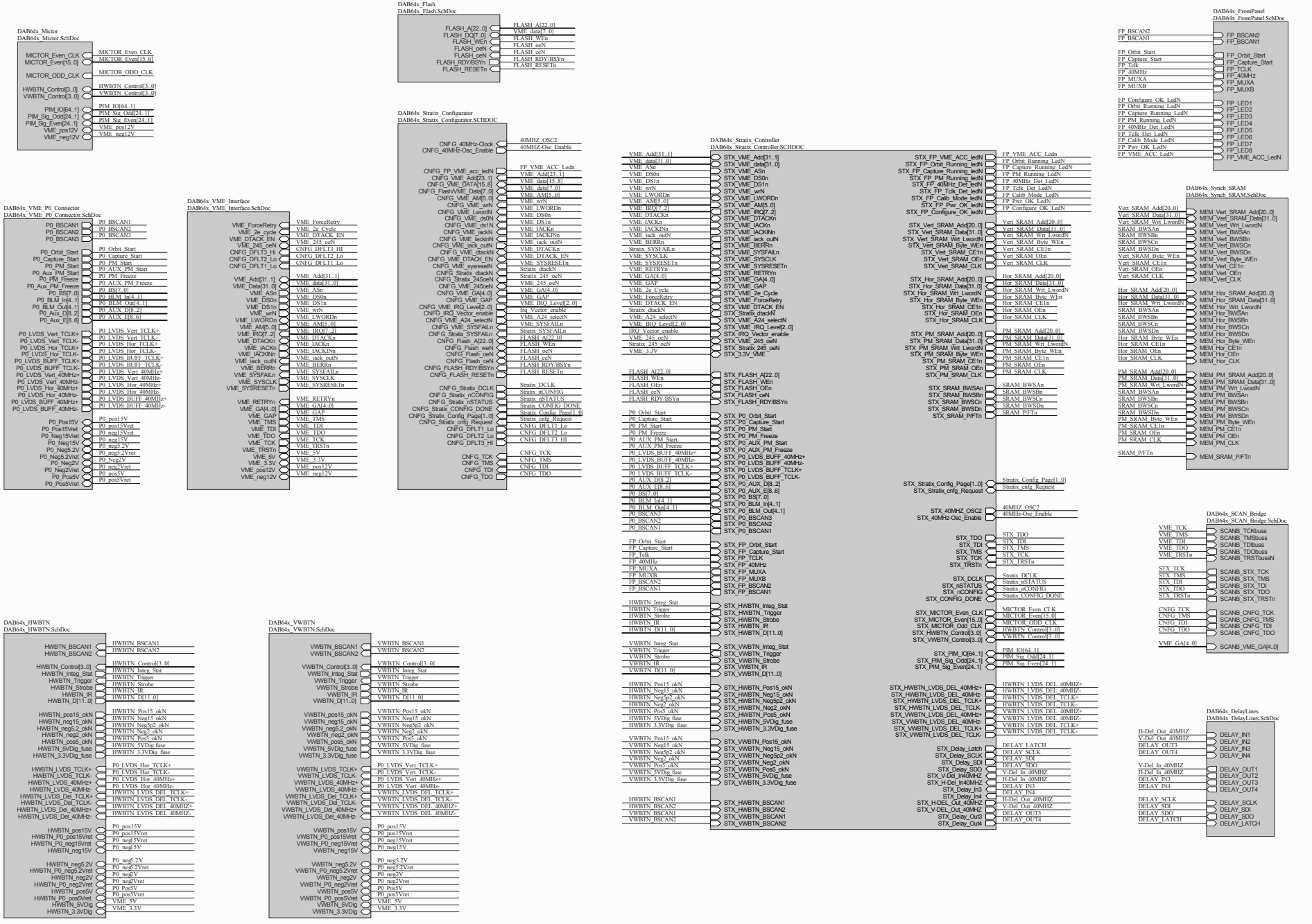
DAB64x_Mictor
DAB64x_Mictor.SchDoc
MICTOR_Even_CLK
MICTOR_Even[15..0]
MICTOR_ODD_CLK
HWBTN_Control[3..0]
VWBTN_Control[3..0]
PIM_IO[64..1]
PIM_Sig_Odd[24..1]
PIM_Sig_Even[24..1]
VME_pos12V
VME_neg12V
DAB64x_Flash
DAB64x_Flash.SchDoc
FLASH_A[22..0]
FLASH_DQ[7..0]
FLASH_WEn
FLASH_oeN
FLASH_ceN
FLASH_RDY/BSYn
FLASH_RESETn
DAB64x_Stratix_Configurator
DAB64x_Stratix_Configurator.SCHDOC
CNFG_40MHz-Clock
CNFG_40MHZ-Osc_Enable
40MHZ_OSC2
40MHZ-Osc_Enable
CNFG_FP_VME_acc_ledN
CNFG_VME_Add[23..1]
CNFG_VME_DATA[15..8]
CNFG_Flash/VME_Data[7..0]
CNFG_VME_AM[5..0]
CNFG_VME_wrN
CNFG_VME_LwordN
CNFG_VME_dsON
CNFG_VME_ds1N
CNFG_VME_lackN
CNFG_VME_lackinN
CNFG_VME_iack_outN
CNFG_VME_dtackN
CNFG_VME_DTACK_EN
CNFG_VME_sysresetN
CNFG_Stratix_dtackN
CNFG_Stratix_245oeN
CNFG_VME_245oeN
CNFG_VME_GA[4..0]
CNFG_VME_GAP
CNFG_VME_IRQ_Level[2..0]
CNFG_IRQ_Vector_enable
CNFG_VME_A24_selectN
CNFG_VME_SYSFAILn
CNFG_Stratix_SYSFAILn
CNFG_Flash_A[22..0]
CNFG_Flash_weN
CNFG_Flash_oeN
CNFG_Flash_ceN
CNFG_FLASH_RDY/BSYn
CNFG_FLASH_RESETn
CNFG_Stratix_DCLK
CNFG_Stratix_nCONFIG
CNFG_Stratix_nSTATUS
CNFG_Stratix_CONFIG_DONE
CNFG_Stratix_Config_Page[1..0]
CNFG_Stratix_cnfg_Request
CNFG_DFLT1_Lo
CNFG_DFLT2_Lo
CNFG_DFLT3_HI
CNFG_TCK
CNFG_TMS
CNFG_TDI
CNFG_TDO
FP_VME_ACC_Ledn
VME_Add[23..1]
VME_data[15..8]
VME_data[7..0]
VME_AM[5..0]
VME_wrN
VME_LWORDn
VME_DS0n
VME_DS1n
VME_IACKn
VME_IACKINn
VME_iack_outN
VME_DTACKn
VME_DTACK_EN
VME_SYSRESETn
Stratix_dtackN
Stratix_245_oeN
VME_245_oeN
VME_GA[4..0]
VME_GAP
VME_2e_Cycle
VME_ForceRetry
VME_DTACK_EN
VME_A24_selectN
VME_IRQ_Level[2..0]
IRQ_Vector_enable
VME_245_oeN
Stratix_245_oeN
VME_3.3V
DAB64x_Stratix_Controller
DAB64x_Stratix_Controller.SCHDOC
VME_Add[31..1]
VME_data[31..0]
VME_ASn
VME_DS0n
VME_DS1n
VME_wrN
VME_LWORDn
VME_AM[5..0]
VME_IRQ[7..2]
VME_DTACKn
VME_IACKn
VME_IACKINn
VME_iack_outN
VME_BERRn
Stratix_SYSFAILn
VME_SYSCLK
VME_SYSRESETn
VME_RETRYn
VME_GA[4..0]
VME_GAP
VME_2e_Cycle
VME_ForceRetry
VME_DTACK_EN
VME_A24_selectN
VME_IRQ_Level[2..0]
IRQ_Vector_enable
VME_245_oeN
Stratix_245_oeN
VME_3.3V
FLASH_A[22..0]
FLASH_WEn
FLASH_OEn
FLASH_ceN
FLASH_RDY/BSYn
P0_Orbit_Start
P0_Capture_Start
P0_PM_Start
P0_PM_Freeze
P0_AUX_PM_Start
P0_LVDS_BUFF_40MHz+
P0_LVDS_BUFF_40MHz-
P0_LVDS_BUFF_TCLK+
P0_LVDS_BUFF_TCLK-
P0_AUX_D[8..2]
P0_AUX_E[8..6]
P0_BS[7..0]
P0_BLM_In[4..1]
P0_BLM_Out[4..1]
P0_BSCAN3
P0_BSCAN2
P0_BSCAN1
FP_Orbit_Start
FP_Capture_Start
FP_Tclk
FP_40MHz
FP_MUXA
FP_MUXB
FP_BSCAN2
FP_BSCAN1
HWBTN_Integ_Stat
HWBTN_Trigger
HWBTN_Strobe
HWBTN_IR
HWBTN_D[11..0]
VWBTN_Integ_Stat
VWBTN_Trigger
VWBTN_Strobe
VWBTN_IR
VWBTN_D[11..0]
HWBTN_Pos15_okN
HWBTN_Neg15_okN
HWBTN_Neg5p2_okN
HWBTN_Neg2_okN
HWBTN_Pos5_okN
HWBTN_5VDig_fuse
HWBTN_3.3VDig_fuse
VWBTN_Pos15_okN
VWBTN_Neg15_okN
VWBTN_Neg5p2_okN
VWBTN_Neg2_okN
VWBTN_Pos5_okN
VWBTN_5VDig_fuse
VWBTN_3.3VDig_fuse
HWBTN_BSCAN1
HWBTN_BSCAN2
VWBTN_BSCAN1
VWBTN_BSCAN2
STX_FP_VME_ACC_ledN
STX_FP_Orbit_Running_ledN
STX_FP_Capture_Running_ledN
STX_FP_PM_Running_ledN
STX_FP_40MHz_Det_ledN
STX_FP_Tclk_Det_ledN
STX_FP_Calib_Mode_ledN
STX_FP_Pwr_OK_ledN
STX_FP_Configure_OK_ledN
STX_Vert_SRAM_Add[20..0]
STX_Vert_SRAM_Data[31..0]
STX_Vert_SRAM_Wrt_LwordN
STX_Vert_SRAM_Byte_WEn
STX_Vert_SRAM_CE1n
STX_Vert_SRAM_OEn
STX_Vert_SRAM_CLK
STX_Hor_SRAM_Add[20..0]
STX_Hor_SRAM_Data[31..0]
STX_Hor_SRAM_Wrt_LwordN
STX_Hor_SRAM_Byte_WEn
STX_Hor_SRAM_CE1n
STX_Hor_SRAM_OEn
STX_Hor_SRAM_CLK
STX_PM_SRAM_Add[20..0]
STX_PM_SRAM_Data[31..0]
STX_PM_SRAM_Wrt_LwordN
STX_PM_SRAM_Byte_WEn
STX_PM_SRAM_CE1n
STX_PM_SRAM_OEn
STX_PM_SRAM_CLK
STX_SRAM_BWSAn
STX_SRAM_BWSBn
STX_SRAM_BWSCn
STX_SRAM_BWSDn
STX_SRAM_P/FTn
STX_Stratix_Config_Page[1..0]
STX_Stratix_cnfg_Request
STX_40MHZ_OSC2
STX_40MHz-Osc_Enable
STX_TDO
STX_TDI
STX_TMS
STX_TCK
STX_TRSTn
STX_DCLK
STX_nSTATUS
STX_nCONFIG
STX_CONFIG_DONE
STX_MICTOR_Even_CLK
STX_MICTOR_Even[15..0]
STX_MICTOR_Odd_CLK
STX_HWBTN_Control[3..0]
STX_VWBTN_Control[3..0]
STX_PIM_IO[64..1]
STX_PIM_Sig_Odd[24..1]
STX_PIM_Sig_Even[24..1]
STX_HWBTN_LVDS_DEL_40MHz+
STX_HWBTN_LVDS_DEL_40MHz-
STX_HWBTN_LVDS_DEL_TCLK+
STX_HWBTN_LVDS_DEL_TCLK-
STX_VWBTN_LVDS_DEL_40MHz+
STX_VWBTN_LVDS_DEL_40MHz-
STX_VWBTN_LVDS_DEL_TCLK+
STX_VWBTN_LVDS_DEL_TCLK-
STX_Delay_Latch
STX_Delay_SCLK
STX_Delay_SDI
STX_Delay_SDO
STX_V-Del_In40MHZ
STX_H-Del_In40MHZ
STX_Delay_In3
STX_Delay_In4
STX_H-DEL_Out_40MHZ
STX_V-DEL_Out_40MHZ
STX_Delay_Out3
STX_Delay_Out4
DAB64x_FrontPanel
DAB64x_FrontPanel.SchDoc
FP_BSCAN2
FP_BSCAN1
FP_Orbit_Start
FP_Capture_Start
FP_Tclk
FP_40MHz
FP_MUXA
FP_MUXB
FP_Configure_OK_LedN
FP_Orbit_Running_LedN
FP_Capture_Running_LedN
FP_PM_Running_LedN
FP_40MHz_Det_LedN
FP_Tclk_Det_LedN
FP_Calib_Mode_LedN
FP_PWR_OK_LedN
FP_Configure_OK_LedN
FP_VME_ACC_LedN
FP_LED1
FP_LED2
FP_LED3
FP_LED4
FP_LED5
FP_LED6
FP_LED7
FP_LED8
FP_VME_ACC_LedN
DAB64x_Synch_SRAM
DAB64x_Synch_SRAM.SchDoc
Vert_SRAM_Add[20..0]
Vert_SRAM_Data[31..0]
Vert_SRAM_Wrt_LwordN
SRAM_BWSAn
SRAM_BWSBn
SRAM_BWSCn
SRAM_BWSDn
Vert_SRAM_Byte_WEn
Vert_SRAM_CE1n
Vert_SRAM_OEn
Vert_SRAM_CLK
Hor_SRAM_Add[20..0]
Hor_SRAM_Data[31..0]
Hor_SRAM_Wrt_LwordN
Hor_SRAM_Byte_WEn
Hor_SRAM_CE1n
Hor_SRAM_OEn
Hor_SRAM_CLK
PM_SRAM_Add[20..0]
PM_SRAM_Data[31..0]
PM_SRAM_Wrt_LwordN
PM_SRAM_Byte_WEn
PM_SRAM_CE1n
PM_SRAM_OEn
PM_SRAM_CLK
SRAM_P/FTn
MEM_Vert_SRAM_Add[20..0]
MEM_Vert_SRAM_Data[31..0]
MEM_Vert_Wrt_LwordN
MEM_Vert_BWSAn
MEM_Vert_BWSBn
MEM_Vert_BWSCn
MEM_Vert_BWSDn
MEM_Vert_Byte_WEn
MEM_Vert_CE1n
MEM_Vert_OEn
MEM_Vert_CLK
MEM_Hor_SRAM_Add[20..0]
MEM_Hor_SRAM_Data[31..0]
MEM_Hor_Wrt_LwordN
MEM_Hor_BWSAn
MEM_Hor_BWSBn
MEM_Hor_BWSCn
MEM_Hor_BWSDn
MEM_Hor_Byte_WEn
MEM_Hor_CE1n
MEM_Hor_OEn
MEM_Hor_CLK
MEM_PM_SRAM_Add[20..0]
MEM_PM_SRAM_Data[31..0]
MEM_PM_Wrt_LwordN
MEM_PM_BWSAn
MEM_PM_BWSBn
MEM_PM_BWSCn
MEM_PM_BWSDn
MEM_PM_Byte_WEn
MEM_PM_CE1n
MEM_PM_OEn
MEM_PM_CLK
MEM_SRAM_P/FTn
DAB64x_SCAN_Bridge
DAB64x_SCAN_Bridge.SchDoc
VME_TCK
VME_TMS
VME_TDI
VME_TDO
VME_TRSTn
SCANB_TCKbuss
SCANB_TMSbuss
SCANB_TDIbuss
SCANB_TDObuss
SCANB_TRSTbussN
STX_TCK
STX_TMS
STX_TDI
STX_TDO
STX_TRSTn
SCANB_STX_TCK
SCANB_STX_TMS
SCANB_STX_TDI
SCANB_STX_TDO
SCANB_STX_TRSTn
CNFG_TCK
CNFG_TMS
CNFG_TDI
CNFG_TDO
SCANB_CNFG_TCK
SCANB_CNFG_TMS
SCANB_CNFG_TDI
SCANB_CNFG_TDO
VME_GA[4..0]
SCANB_VME_GA[4..0]
DAB64x_DelayLines
DAB64x_DelayLines.SchDoc
H-Del_Out_40MHZ
V-Del_Out_40MHZ
DELAY_OUT3
DELAY_OUT4
DELAY_IN1
DELAY_IN2
DELAY_IN3
DELAY_IN4
V-Del_In 40MHZ
H-Del_In 40MHZ
DELAY_IN3
DELAY_IN4
DELAY_OUT1
DELAY_OUT2
DELAY_OUT3
DELAY_OUT4
DELAY_SCLK
DELAY_SDI
DELAY_SDO
DELAY_LATCH
DAB64x_VME_P0_Connector
DAB64x_VME_P0_Connector.SchDoc
P0_BSCAN1
P0_BSCAN2
P0_BSCAN3
P0_Orbit_Start
P0_Capture_Start
P0_PM_Start
P0_Aux_PM_Start
P0_PM_Freeze
P0_Aux_PM_Freeze
P0_BS[7..0]
P0_BLM_In[4..1]
P0_BLM_Out[4..1]
P0_Aux_D[8..2]
P0_Aux_E[8..6]
P0_LVDS_Vert_TCLK+
P0_LVDS_Vert_TCLK-
P0_LVDS_Hor_TCLK+
P0_LVDS_Hor_TCLK-
P0_LVDS_BUFF_TCLK+
P0_LVDS_BUFF_TCLK-
P0_LVDS_Vert_40MHz+
P0_LVDS_Vert_40MHz-
P0_LVDS_Hor_40MHz+
P0_LVDS_Hor_40MHz-
P0_LVDS_BUFF_40MHz+
P0_LVDS_BUFF_40MHz-
P0_pos15V
P0_pos15Vret
P0_neg15Vret
P0_neg15V
P0_neg5.2V
P0_neg5.2Vret
P0_Neg2V
P0_neg2Vret
P0_pos5V
P0_pos5Vret
DAB64x_VME_Interface
DAB64x_VME_Interface.SchDoc
VME_ForceRetry
VME_2e_cycle
VME_DTACK_EN
VME_245_oeN
CNFG_DFLT3_Hi
CNFG_DFLT2_Lo
CNFG_DFLT1_Lo
VME_Add[31..1]
VME_Data[31..0]
VME_ASn
VME_DS0n
VME_DS1n
VME_wrN
VME_LWORDn
VME_AM[5..0]
VME_IRQ[7..2]
VME_DTACKn
VME_IACKn
VME_IACKINn
VME_iack_outN
VME_BERRn
VME_SYSFAILn
VME_SYSCLK
VME_SYSRESETn
VME_RETRYn
VME_GA[4..0]
VME_GAP
VME_TMS
VME_TDI
VME_TDO
VME_TCK
VME_TRSTn
VME_5V
VME_3.3V
VME_pos12V
VME_neg12V
DAB64x_HWBTN
DAB64x_HWBTN.SchDoc
HWBTN_BSCAN1
HWBTN_BSCAN2
HWBTN_Control[3..0]
HWBTN_Integ_Stat
HWBTN_Trigger
HWBTN_Strobe
HWBTN_IR
HWBTN_D[11..0]
HWBTN_Pos15_okN
HWBTN_Neg15_okN
HWBTN_Neg5p2_okN
HWBTN_Neg2_okN
HWBTN_Pos5_okN
HWBTN_5VDig_fuse
HWBTN_3.3VDig_fuse
HWBTN_LVDS_TCLK+
HWBTN_LVDS_TCLK-
HWBTN_LVDS_40MHz+
HWBTN_LVDS_40MHz-
HWBTN_LVDS_Del_TCLK+
HWBTN_LVDS_Del_TCLK-
HWBTN_LVDS_Del_40MHz+
HWBTN_LVDS_Del_40MHz-
HWBTN_pos15V
HWBTN_P0_pos15Vret
HWBTN_P0_neg15Vret
HWBTN_neg15V
HWBTN_neg5.2V
HWBTN_P0_neg5.2Vret
HWBTN_neg2V
HWBTN_P0_neg2Vret
HWBTN_pos5V
HWBTN_P0_pos5Vret
HWBTN_5VDig
HWBTN_3.3VDig
DAB64x_VWBTN
DAB64x_VWBTN.SchDoc
VWBTN_BSCAN1
VWBTN_BSCAN2
VWBTN_Control[3..0]
VWBTN_Integ_Stat
VWBTN_Trigger
VWBTN_Strobe
VWBTN_IR
VWBTN_D[11..0]
VWBTN_Pos15_okN
VWBTN_Neg15_okN
VWBTN_Neg5p2_okN
VWBTN_Neg2_okN
VWBTN_Pos5_okN
VWBTN_5VDig_fuse
VWBTN_3.3VDig_fuse
VWBTN_LVDS_TCLK+
VWBTN_LVDS_TCLK-
VWBTN_LVDS_40MHz+
VWBTN_LVDS_40MHz-
VWBTN_LVDS_Del_TCLK+
VWBTN_LVDS_Del_TCLK-
VWBTN_LVDS_Del_40MHz+
VWBTN_LVDS_Del_40MHz-
VWBTN_pos15V
VWBTN_P0_pos15Vret
VWBTN_P0_neg15Vret
VWBTN_neg15V
VWBTN_neg5.2V
VWBTN_P0_neg5.2Vret
VWBTN_neg2V
VWBTN_P0_neg2Vret
VWBTN_pos5V
VWBTN_P0_pos5Vret
VWBTN_5VDig
VWBTN_3.3VDig
DAB64x MODULE
Revision
0
Drawing #:
Sheet#: 1 of 13
Size: C
Drawn by: TRIUMF
Date: 03/06/2004
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
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V6T 2A3
Cannot open file G:\AHW\PROTEL\SCH
File: C:\AHW\CERN\DAB64x\Protel-DXP\DAB64xModule.SchDoc
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