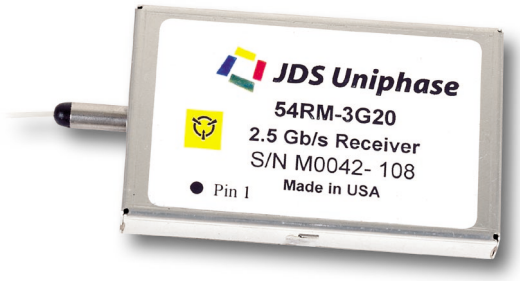
JDS Uniphase

Product Bulletin



45 Mb/s to 2.7 Gb/s Optical Receiver Module

54RM Series

The JDS Uniphase 54RM series receiver module is designed for use in telecommunications systems and high speed data communications applications. It is optimized for SONET OC-48 and synchronous digital hierarchy (SDH) STM-16 line interfaces. Its uniform package, pin function, and common optical and electrical characteristics are multisource agreement (MSA) compliant.

The 54RM 3R receiver design incorporates an Indium Gallium Arsenide (InGaAs) Avalanche photodiode (APD) detector, and full clock and data recovery (CDR) regeneration. It contains an integrated APD high voltage supply that is temperature-compensated at our factory for optimum sensitivity. The 54 RM 3R receiver module operates with 54TM and 57TM transmitters.

The 54RM 2R receiver design incorporates an InGaAs APD detector but does not include a CDR function, thus allowing additional system design flexibility. The 2R receiver module operates at continuous rates from 45 Mb/s to 2.7 Gb/s without gap and provides options for current mode logic (CML) or LVPECL outputs. The 2R receiver also features an optical input level voltage (OILV) monitor with ±1dB accuracy and decision threshold voltage (DTV) adjustment.

Key Features

- MSA compliant
- Optimized for SONET OC-48 and SDH STM-16 (54RM 3R version)
- 1310 nm or 1550 nm operation
- Data rates from 45 Mb/s to 2.7 Gb/s for 2R configuration
- APD for better than -30 dBm sensitivity
- -40 °C to 85 °C operation

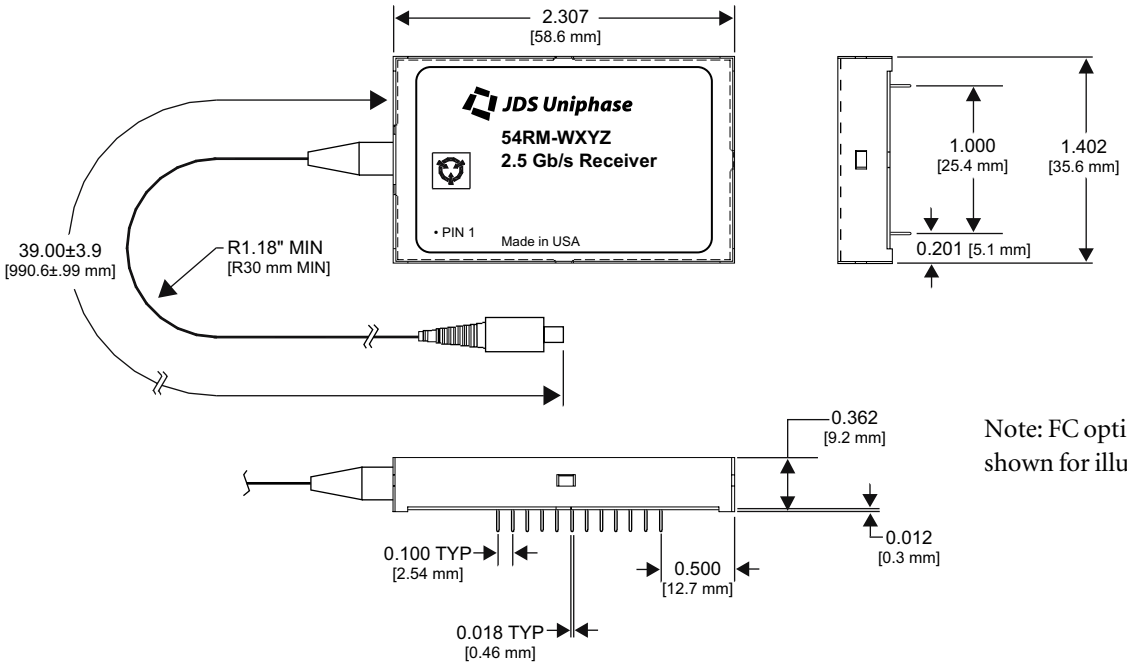
Applications

- High speed, long haul fiberoptic links for voice, data, and digital video
- Metropolitan area networks
- Wide area networks

Compliance

- Telcordia GR-253-CORE
- ITU-T G.958

Dimensions Diagram (Specifications in inches [mm].)



Note: FC optical connectors are shown for illustration only.

Pinout

Pin	Symbol	Description
1	NIC	No internal connection
2	NUC	No user connection
3	LPA	Loss of power alarm[1]
4	GND	Ground[2]
5	CLKout/ NIC	False clock output[3]
6	CLKout/ NIC	True clock output[3]
7	GND	Ground[2]
8	VCC	Positive power supply
9	GND	Ground[2]
10	Dout	True data output
11	Dout	False data output
12	GND	Ground[2]
13	DTV/NIC	Decision threshold voltage/no internal connection[4]
14	GND	Ground[2]
15	GND	Ground[2]
16	GND	Ground[2]
17	GND	Ground[2]
18	NIC	No internal connection
19	GND	Ground[2]
20	GND	Ground[2]
21	NUC	No user connection/I2C serial data
22	VCC	Positive power supply
23	OILV / NIC	Optical input level voltage /No internal connection[5]
24	NUC	No user connection/I2C serial clock

1. LPA output is a logic level that indicates the presence or absence of a sufficient optical input level. A logical high level indicates an input optical level that is too low.
2. Package is at the same potential as GND.
3. These pins are configured as No Internal Connection for the 54RM-4XYZ version. The CLKout signals are provided on these pins for the 54RM-3XYZ.
4. This pin is configured as NIC for the 54RM-3XYZ version and configured as the Decision Threshold Voltage (DTV) for the 54RM-4XYZ version. See separate application note for a description of the DTV input, if the DTV function is not required, pin 13 should be left open.
5. This pin is configured as NIC for the 54RM-3XYZ and configured as the OILV monitor for the 54RM-4XYZ.

Optical Specifications[1]

Parameter		54RM-WXYZ (1310 nm)			54RM-WXYZ (1550 nm)		
	Symbol	Minimum	Typical	Maximum	Minimum	Typical	Maximum
ITU-T/SONET		-	L-16.1 / LR-1	-	-	L-16.2 / LR-2	-
Optical budget[2]		10 dB	-	24 dB	10 dB	-	24 dB
Center wavelength	λ_c	1260 nm	-	1335 nm	1500 nm	-	1620 nm
Receiver sensitivity[3,4]	Psens	-27.5 dBm	-30 dBm	-	-28.5 dBm	-31 dBm	-
Receiver overload[3]	Povld	-8 dBm	-7 dBm	-	-8 dBm	-7 dBm	-
Maximum input power[5]	Pmax	1 dBm	2 dBm	-	1 dBm	2 dBm	-
Maximum reflectance		-	-28 dB	-27 dB	-	-28 dB	-27 dB

1. All minimum and maximum parameters are specified end-of-life within the overall, relevant operating temperature range. The typical values are referenced to 25 °C (nominal power supply) beginning of life. The operating conditions are: Vcc = 4.75 to 5.25 V DC
   Vee = 0 V DC
   Line bit rate: 2.48832 Gbps ±20 ppm
   Line code: SONET STS-48 frame with scrambler, with PRBS23 payload
   Line extinction ratio ≥8.2 dB
   BER ≤$1x10^{-10}$
2. The V-16.2 version is adapted to standard 10 to 13 dBm EDFA optical bandwidth.
3. Measured at BER 10^{-10} at EOL.
4. Measured at connector interface.
5. Operation above this input power could damage the device.

Electrical Specifications

Parameters		Symbol	Minimum	Typical	Maximum
Positive supply voltage			4.75 V	5 V	5.25 V
APD HV supply			Internal	-	-
Power consumption			-	1.7 W	2.5 W
Output data and clock voltage differential[1]		DV	0.6 V_{p-p}	-	1.6 V_{p-p}
Output rise time (20 % to 80 %)		Tr	-	-	150 ps
Output fall time (80 % to 20 %)		Tf	-	-	150 ps
Data output jitter p-p [1]		J	-	-	20 ps
Output clock and data return loss[1]	Clock (1 to 2 GHz)	RL(C)	6 dB	-	-
	Clock (2 to 2.8 GHz)		12 dB	-	-
	Data (1 to 1 GHz)	RL(D)	12 dB	-	-
	Data (1 to 2 GHz)		9 dB	-	-
	Data (2 to 2.5 GHz)		6 dB	-	-
Loss of power alarm output level: normal signal input[2]		LPA	0 V	-	0.4 V
Loss of power alarm output level: low signal input (alarm)[2]		Llite	2.4 V	-	Vcc
"Low Light" alarm assert time[2]		T(aa)	-	-	1 ms
"Low Light" alarm de-assert time[2]		T(a0)	-	-	1 ms
Clock and data differential skew[3]		Dtout	-	-	20 ps
Clock duty cycle[4]			45%	-	55%
Maximum receive clock frequency drift (with no light input)			-	-	100 MHz
Data, clock load drive capability[5]		R_L			
Consecutive identical bits[6]		CID	-	-	72 bits
Jitter generation				Meets GR-253/ITU-T G.958	
Jitter tolerance				Meets GR-253/ITU-T G.958	
Jitter transfer				Meets GR-253/ITU-T G.958	
Logic output level				TTL compatible	

1. Must be externally AC coupled and externally loaded by 50 Ω. Applies only to 3R version.
2. Squelching of data and clock is NOT allowed when alarm is active.
3. This skew is the 'p' to 'n' skew of the differential data signals and clock signals. Applies only to 3R version.
4. No skipped clock cycles allowed down to less than $1x10^{-3}$ BER. (i.e., no PLL cycle slipping).
5. Externally AC coupled, terminated into 50 Ω.
6. The receiver must tolerate a minimum of 72 clock periods of no data (light) transitions and still meet output clock jitter requirements and have no misclocking of data.

Ordering Information

For more information on this or other products and their availability, please contact your local JDS Uniphase account manager or JDS Uniphase directly at 800-871-8537 in North America and 800-8735-5378 worldwide or via e-mail at jdsu.sales@jdsu.com.

Sample: 54RM-3G20

54RM- □ □ □ □

Code	Photodetector
3	APD with CDR
4	APD without CDR

Code	Connector Type
C	ST/SPC
D	FC/SPC
G	SC/SPC
L	LC/SPC
M	MU/SPC

Code	Class
1	-5 to 75 °C
2	-40 to 85 °C

Code	Adapter
0	No adapter, CML output
1	With adapter
2	LVPECL output, external termination
3	LVPECL output, internal termination

Note: Adapter card is a 2x4 in PCB which provides a necessary form factor adjustment for a specific customer. CML or LVPECL output levels are selectable only for the 2R version (without CDR).

JDS Uniphase

North America toll-free: 800-871-8537
Worldwide toll-free: 800-8735-5378
www.jdsu.com

10134445 Rev. 001 03/02