ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE
EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

Laboratoire Européen pour la Physique des Particules
European Laboratory for Particle Physics

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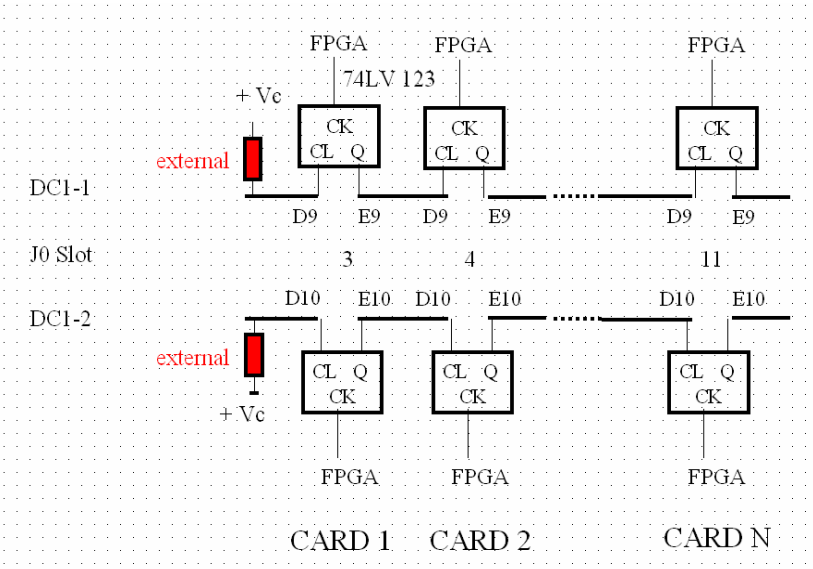
TEST OF THE DAB REV2 V2 DAISY CHAIN

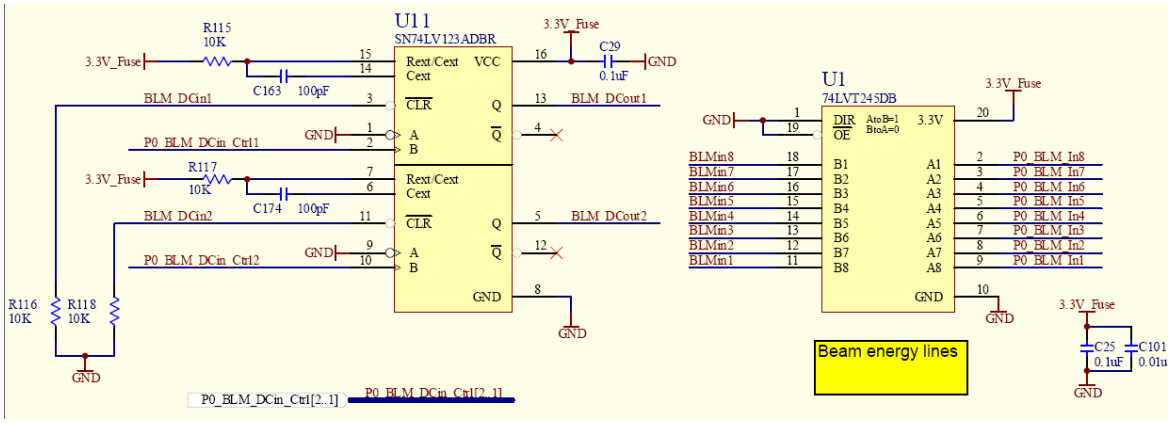
See also Tech. Spec VME Create (EDMS 365170)

The principle of the daisy chain in the DAB is shown in the figure below.

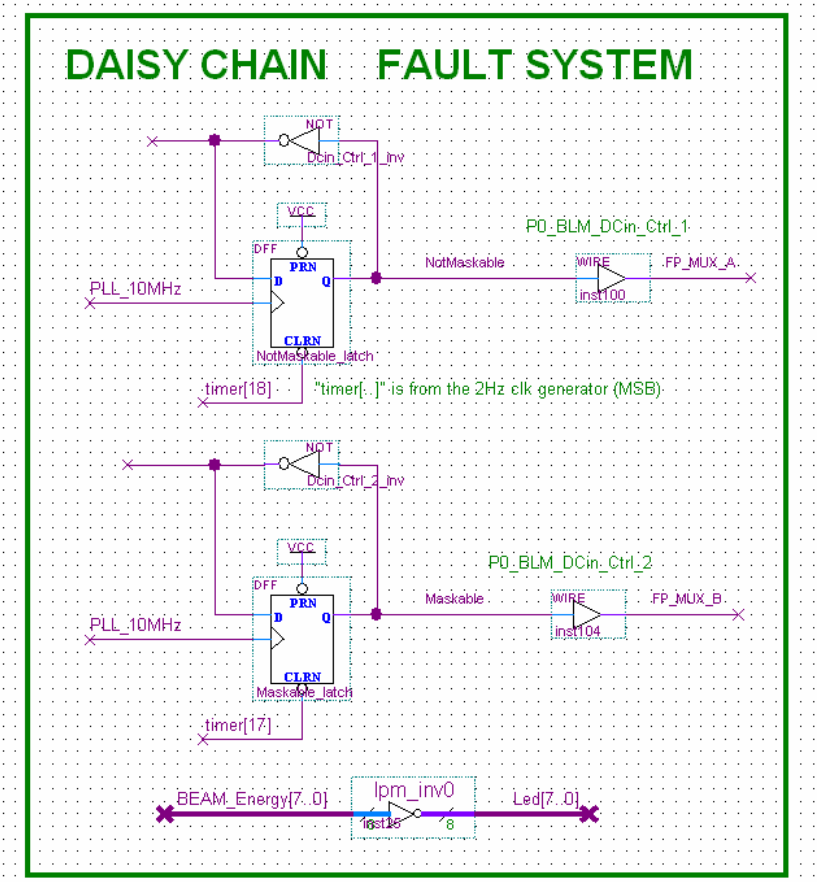


The pull-up at the beginning of the line gives a '1' to the first 'CL' (active low). Then the 'CK' input must be feed with a frequency to retrigger the internal timer and maintain the '1' to the output 'Q'. If one of the card is removed or the FPGA stop sending the frequency to the 'CK' input, the line goes to '0' and arrive to the combiner card.

Schematic of the function on the new DAB rev2 v2:

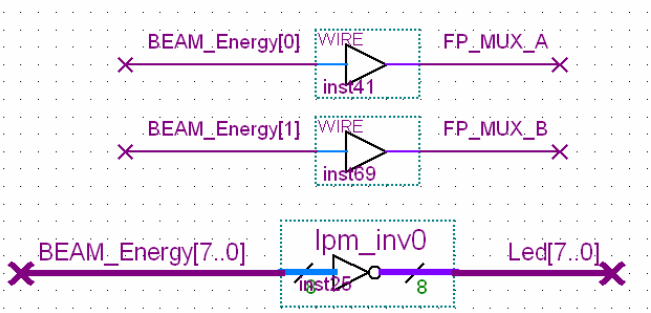


Schematic of the FPGA description for the Daisy chain test



In this design, the signals (timer[x]) enable and disable constantly (2Hz and 4Hz) the frequency generators used to hold the lines (BLM_DCountx) high thought the multvibrator. The result on the P0 connector (and the measurements described below) is a constant variation of these 2 signals (high-low-high..) of 2Hz (nonmaskable) and 4 Hz (masskable). See also test 2.

Schematic of the FPGA description for the Beam Energy lines



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Connector P0 with the interesting lines highlighted
from Tech. Spec VME Create (EDMS 365170)

Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	Bus line-0	-5V2RET	-5V2RET	HW Low Byte 1 bit 0	HW High Byte 1 bit 0	GND
2	GND	Bus line-1	-5V2RET	-5V2RET	HW Low Byte 1 bit 1	HW High Byte 1 bit 1	GND
3	GND	Bus line-2	-5V2RET	-5V2RET	HW Low Byte 1 bit 2	HW High Byte 1 bit 2	GND
4	GND	Bus line-3	-5V2	-5V2	HW Low Byte 1 bit 3	HW High Byte 1 bit 3	GND
5	GND	Bus line-4	-5V2	-5V2	HW Low Byte 1 bit 4	HW High Byte 1 bit 4	GND
6	GND	Bus line-5	-5V2	-5V2	HW Low Byte 1 bit 5	HW High Byte 1 bit 5	GND
7	GND	Bus line-6	-2VRET	-2VRET	HW Low Byte 1 bit 6	HW High Byte 1 bit 6	GND
8	GND	Bus line-7	-2VRET	-2VRET	HW Low Byte 1 bit 7	HW High Byte 1 bit 7	GND
9	GND	GPPL-0	-2V	-2V	Daisy chain1- 1-in	Daisy chain1-1-out	GND
10	GND	GPPL-1	-2V	-2V	Daisy chain 1-2-in	Daisy chain 1-2-out	GND
11	GND	GPPL-2	GPPL-3	GPPL-4	GPPL-5	GPPL-6	GND
12	GND	Bus line1-0	+5V	+5V	Bunch Select 1 Bit 0	LVDS Turn clock Delay 1 +	GND
13	GND	Bus line1-1	+5V	+5V	Bunch Select 1 Bit 1	LVDS Turn clock Delay 1 -	GND
14	GND	Bus line1-2	+5VRET	+5VRET	Bunch Select 1 Bit 2	TTL Turn clock Delay 1 +	GND
15	GND	Bus line1-3	+5VRET	+5VRET	Bunch Select 1 Bit 3	TTL Turn clock Delay 1 -	GND
16	GND	Bus line1-4	+15V	+15V	Bunch Select 1 Bit 4	LVDS 40 MHz Clock 1 +	GND
17	GND	Bus line1-5	+15VRET	+15VRET	Bunch Select 1 Bit 5	LVDS 40 MHz Clock 1 -	GND
18	GND	Bus line1-6	-15VRET	-15VRET	Bunch Select 1 Bit 6	TTL 40 MHz Clock 1 +	GND
19	GND	Bus line1-7	-15V	-15V	Bunch Select 1 Bit 7	TTL 40 MHz Clock 1 -	GND

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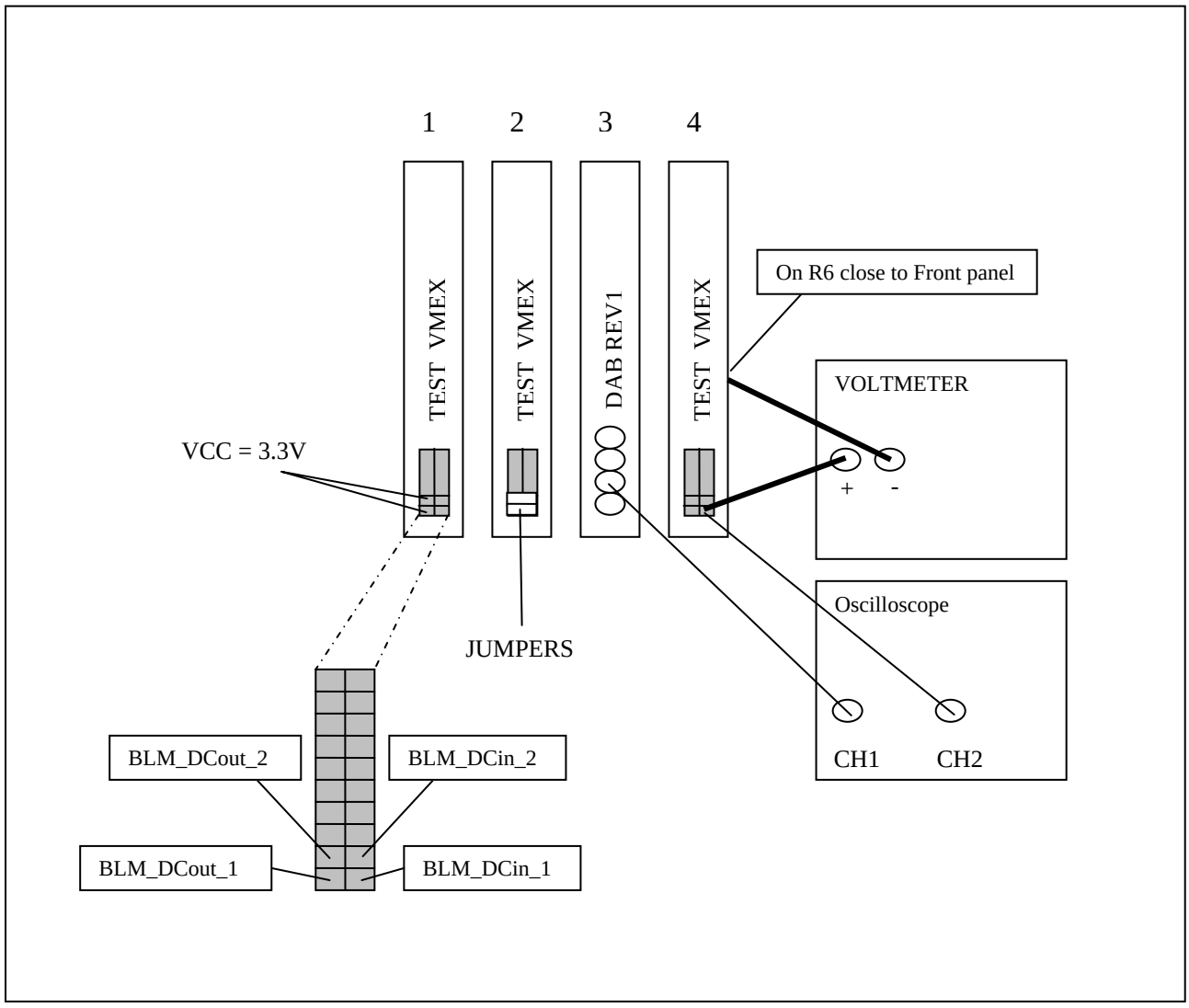
TEST SETUP:



TEST 1:

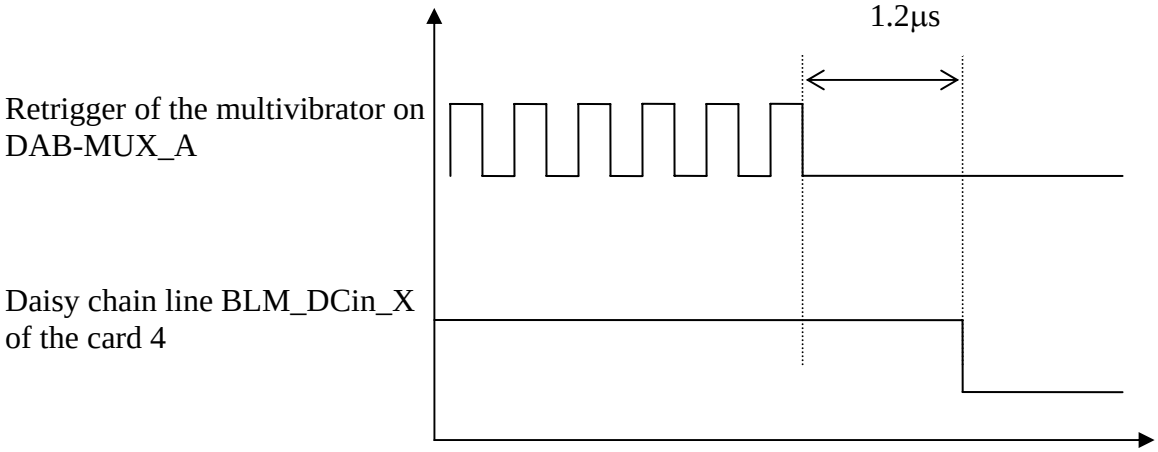
This is a basic test of removing a card which participates to the daisy chain. First apply a 3.3V on the beginning of the chain (Card '1') (Now the create are modified to have that voltages on the slot 4). Then the DAB (Card '3') should be programmed with the appropriate software.

1. Visualise with an oscilloscope the voltage on the card '4' the BLM_DCin 1 and 2, the voltage should be around 3.3V (and pass to 0V then 3.3V with an frequency of 2Hz or 4Hz).
2. Without turn off the vme, remouve the card '2', this will cut the 2 lines. The voltage should be 0V
3. Connect again the card '2', the voltage should be again as point 1).

TEST 2:

This test control the time constant of the multivibrator retriggerable on the DAB card (U11). For that, the FPGA on the DAB is generating the right frequency (higher than 1MHz better 5MHz) for 0.5s and then stop for 0.5s, the cycle will continue indefinitely. The moment that the FPGA stops retrigger the multivibrator with the frequency to the falling of the signal BLM_DCout_x is the interesting timing to measure.

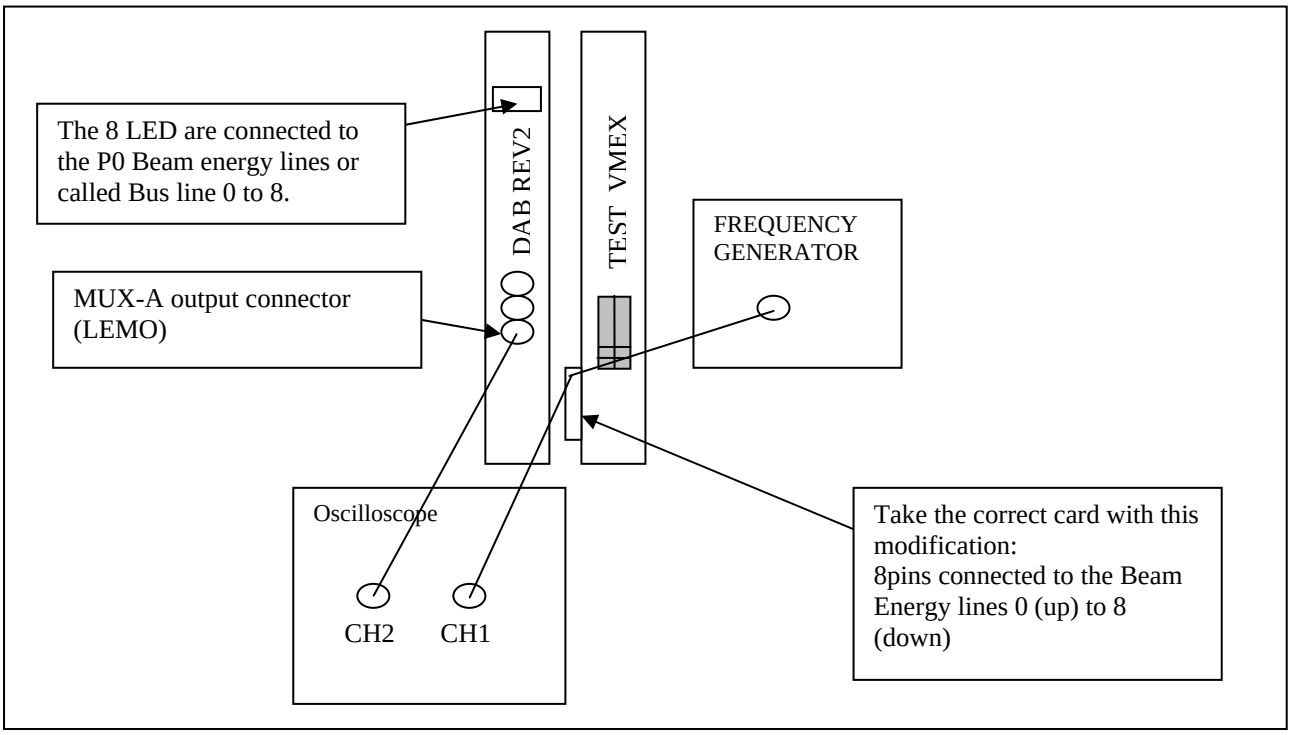
1. Load the FPGA with the appropriate software.
2. Connect the oscilloscope as shown on the figure (TEST SETUP page). Channel 1 to the MUX_A out of the DAB card and the channel 2 on the card '4' signal "BLM_DCin_1".
3. Trig to the falling edge of the channel 2, 5us par division.



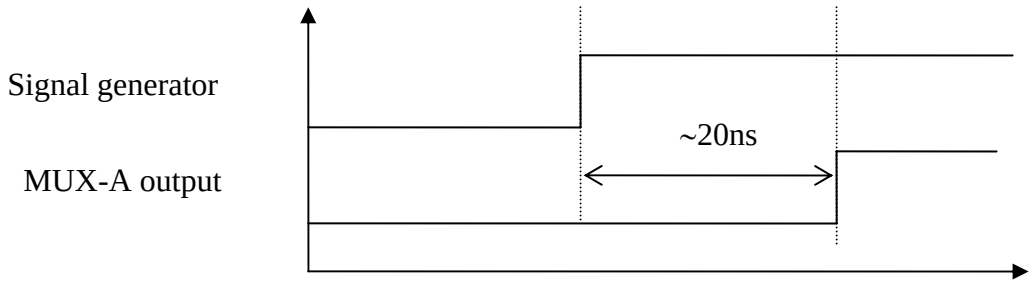
The result must be around 1µs. this timing is quicker that on the Rev1 (was 10us), to speed up the reactivity of the system.

TEST 3:

This test controls the routing and the max frequency usable for the Beam energy lines (called Bus Line 0 to 7 in the document EDMS 365170. For that, these 8 lines are connected to the led on the front panel of the DAB and the first one (Beam Line 0) is connected to the output MUX-A also on the DAB F-P.



1. Load the FPGA with the appropriate software.
2. Apply 0V and then 3.3V on each of the 8 beam energy lines on the board Test VMEX, you should see the effect on the corresponding led of the DAB card.
3. Connect the frequency generator and the oscilloscope as shown. Channel 2 to the MUX_A out of the DAB card and the channel 1 on the Test card signal “Beam energy line 0” (upper pin).
4. Trig to the rising edge of the channel 1, 20ns par division.



Then you can try to find the maximal frequency that passes the channel. The result is around 80ns minimal period. In that range, the lines can not be used because of the bad signal integrity behaviour, but the final use will be much slower.