Projektarbeit

Development of the Analog Front-end for the Beam Loss Monitors of the LHC

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1 Introduction

The Large Hadron Collider (LHC) at the European Laboratory for Particle Physics (CERN) will be the biggest particle accelerator in the world. It will collide two proton beams with an energy of 14 TeV at four intersection points along its 27 km circumference. To generate those high beam energies, superconducting magnets with flux densities up to 8.4 T are used to keep the beams on their track. These magnets become normal conducting if the heat deposition due to particle losses increases their temperature over a critical value. In order to prevent this undesired process and to extract the beam safely (=dump) before a damage takes place, beam loss monitors (BLM) are installed in the tunnel. They measure the particle loss rate and deliver a proportional electric current.

The objective of the internship was to examine the different possibilities for the analog front-end of these beam loss monitors.
This report gives a brief introduction in the beam loss monitors of the LHC. After presenting the specifications and the used sensor for this task, conceptual considerations about monitoring electric current are made. This current constitutes the input signal of the front-end which has to be measured. To optimze the design process we used PSpice to simulate the different circuits before creating a protoype. Several circuits are described and the results of the test series as well as simulation results are presented.

1.1 CERN – The European Organization for Nuclear Research

As one of the first European joint projects, CERN[1] was funded in 1954 near Geneva, Switzerland. The facility is run by 19 European member states and constitutes the largest research center for particle physics in the world. About 6500 scientists from 500 different universities and more than 80 countries use the equipment of CERN [1].
The principal duty of CERN is pure research. Its scientists try to find answers to the basic interaction of matter. Beside the research task, by-products like the computer tomograph, the trackball or the World Wide Web originated at CERN.

[1] Conseil Européen pour la Recherche Nucléaire

Currently the organization is working on the Large Hadron Collider (LHC) which should be launched in 2005. This new particle accelerator will run with unprecedented energies. It will collide two beams of protons at 14 TeV and therefore deliver a deeper insight into matter than ever before. The installation is hosted in the 27 km circumference tunnel of CERN's former Large Electron Positron Collider (LEP). Figure 1 shows CERN's accelerator complex.

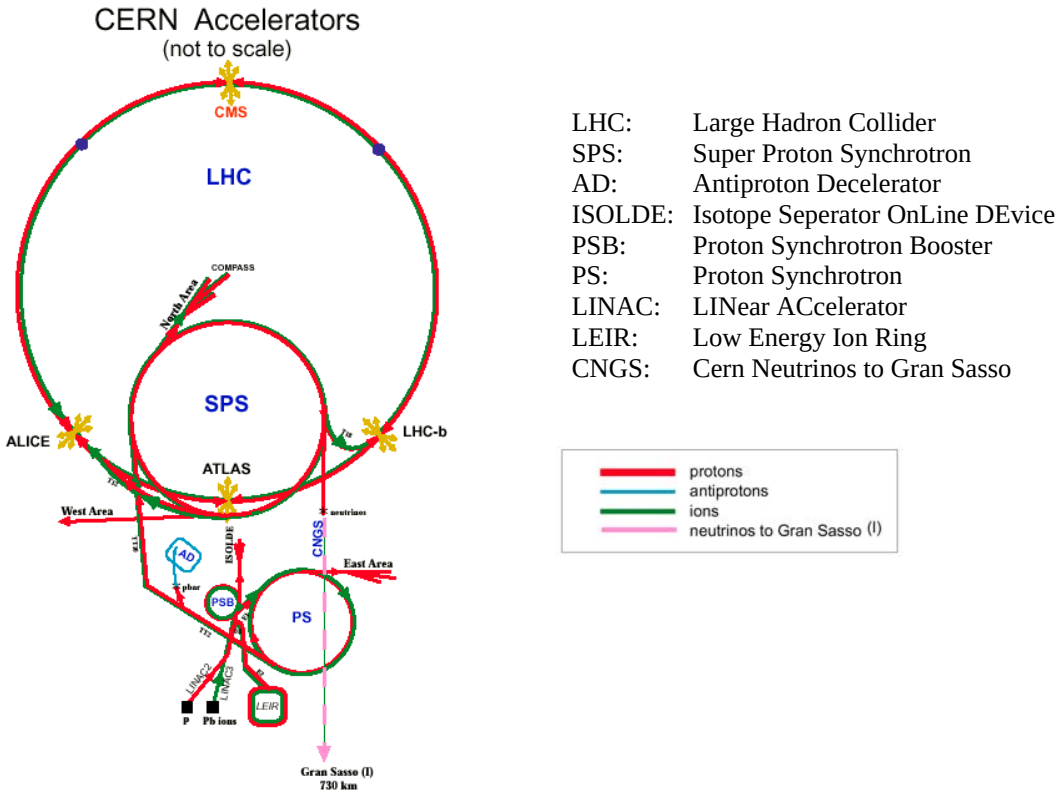


Figure 1 – CERN Accelerators

1.2 The Beam Loss Monitors

The operation of the LHC requires a large variety of instrumentation for the control of the beams, as well as for the control of the protection of the accelerator. Therefore a machine protection system has been developed to minimize the risk of serious damage. The beam loss monitors, which observe the particle losses in the ring, is one part of this facility.

1.2.1 Task of the Beam Loss System

One of the obvious sources of error constitute the superconducting magnets keeping the proton beams on their track. Their total number exceeds 8000. The superconducting coils of

the magnets, operating at 1.2 K, become normal conducting if a heat deposition increases their temperature over a critical value. Heat is deposited in the coil if beam particles leave their nominal orbit and hit the vacuum chamber wall of the beam tube. This proton impact initiates a particle shower which is stopped in the windings of the superconducting coil. The result is a local increase in temperature. This process is called “Quench”.

To protect the magnets from quenching, a protection system has been designed. In the case of a quench the whole string[2] of superconductiong magnets is switched off and uniformly heated up. This method is both costly and means a long time period of no physical experiments since the string must be cooled down to 1.2 K again. To predict a quench and therefore to avoid long off times of the LHC, beam loss monitors are installed in the accelerator tunnel to measure the particle loss rate. This approach is generally used in all particle accelerators – not only at CERN.

There are different kinds of sensors to monitor particle losses. In this report I focus on ionziation chambers since this type is intended to be used for the LHC. These chambers generate an electic current which is proportional to the particle loss rate (Chapter 1.2.2). Figure 2 shows the quench levels of the LHC. They depend on the beam energy as well as on the length of the impact. The thermal conductivity of the surrounding helium flow determines the maximum loss rate at long time intervals. In contrast, at short time intervals the heat reserve of the cables tolerates much higher proton losses.
As one can observe from the diagram, the loss rate extends over a range of 6 decades from 10^7 to 10^{13} proton losses/m/s. This losses have to be measured over a time scale from 0.1 ms to 1000 s [2].

If the proton losses are too high, the beam has to be dumped. In that case a kicker magnet conducts the beam out of the accelerator ring to a block of solid iron. After this extraction a new beam can be injected. For a proper protection the quench levels must not be exceeded, therefore the dump levels are set 50% below the quench levels.

[2] A functional group of magnets.

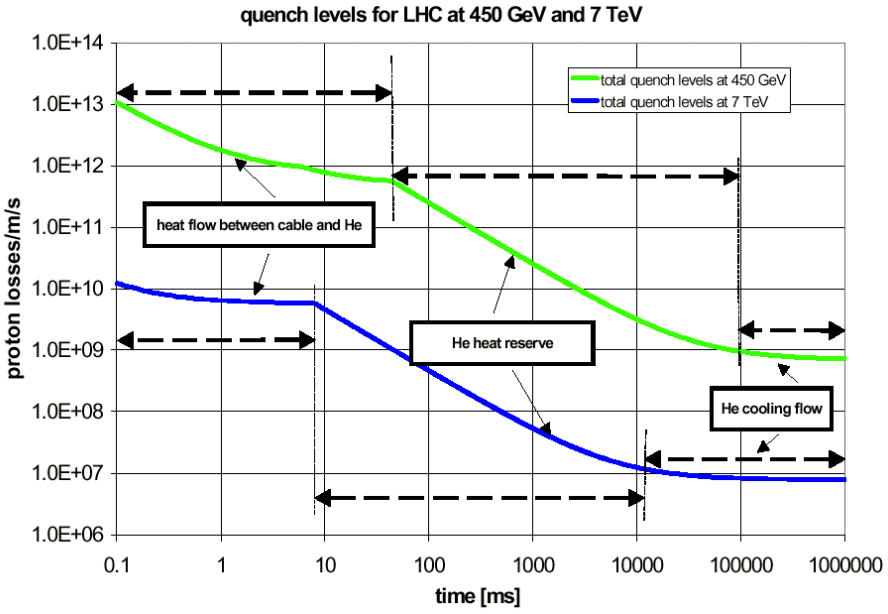
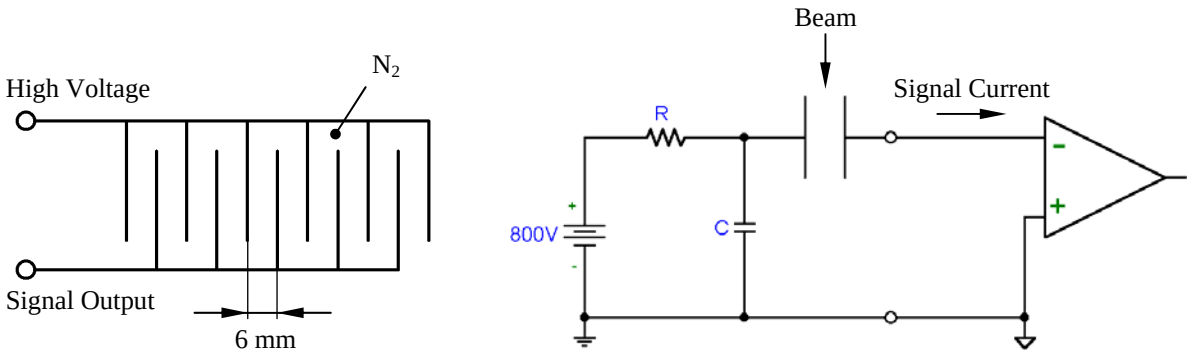


Figure 2 – Quench Levels of the LHC at beam energies of 450GeV and 7TeV [2]

1.2.2 The Ionization Chamber

The ionization chamber constitutes the signal source of the Beam Loss electronic. It converts the particle shower caused by misleaded particles into an electric current. The amplitude is proportional to the loss rate, measured in proton losses per meter and second. The structure is shown in Figure 3. As one can see, the chamber consists of several metal plates connected in parallel. The distance is about 6 mm between each plate. A high electric voltage of 800 V is applied to these rods. The parallel connection increases the total output current but also the capacity. We will see that this capacity plays a certain role in the performance of the circuit. The right part of F

Figure 3 illustrates the connection of the chamber. The bias voltage is applied via a RC



network which provides protection against short cirucits, and ensures a stable bias voltage.

Figure 3 – Schematic of the ionization chamber (left) and connection to the analog front-end electronic (right)

The function of the chamber is based on the principle of ionization. If a particle intrudes the space between two rods, it generates an electron-ion pair. Due to the high voltage between the plates, these charges are separated. The electron is accelerated to the positive plate while the positive ion is attracted by the negative one. This charge separation constitutes an electric current one can measure at the outside connectors. The amplitude of this current depends on the number of intruding particles as well as on the volume of the chamber. A larger number of intruding particles generates more electron-ion pairs and therefore increases the current. On the other side, the bigger the volume the more electron-ion pairs are generated on the particle's way through the chamber. In contrast, the bias voltage doesn't have a significant influence on the amplitude.

1.2.3 Signal Specification

Before we are able to solve our task we have to specify our electronic. The task of this internship was to examine the different possibilities to measure the particle loss rate. Preliminary studies of the ionization chamber show that an output current of 1 mA corresponds to 10^{13} proton losses/m/s. So we set the maximum input current to this value. According to Figure 2 the dynamic range covers 6 decades. To ensure a good sensitivity and to cover uncertainties we have to extend the lower range to 10^{6} proton losses/m/s which leads to a minimum input current of 100 pA at low loss rates. Thus an analog electronic with a dynamic range of 140 dB is required.

We can also take out of Figure 2 that the time interval of the particle impact plays an important role. From the x-axis we observe a minimum measuring time from 100 µs (according the revolution time of the LHC beams of 89 µs) to 1000 s. In this time intervals we have to measure the chamber current, hence they determine the bandwith of our electronic. Preliminary studies revealed that it is possible to predict a quench within an accuracy of ±50%. Therefore the maximum allowable error of the readout electronic has been set to ±10%. The following table summarizes the front-end specifications.

Parameter	Value
Dynamic Range	100 pA – 1 mA
Bandwith	> 10 kHz, depending on the loss rate
SNR	At least 6 dB
Conversion Rate	Min. each Turn = 89 μs
Output Signal	Not specified
Accuracy	±10%

2 Principles of Monitoring Electric Current

Now that all requirements have been considered we could focus on realizing our task. We should be able to detect electric current over a dynamic range of 140 dB with ±10% accuracy between 89 μs and 1000 s respectively. The dynamic range constitutes the most serious problem by far as we will see in the following sections.

2.1 Overview

Since our signal constitutes an electric current, the first step we performed was to search for principles how to measure this one. Figure 4 gives a short overview.

As one can see there are several possibilities to solve the task. We tried to specifiy the basic properties of the circuits in order to make a decision which solution would be worth further investigations.

2.2 Direct Monitoring Techniques

These circuits provide an output which is proportional to the input. The general advantage is that one can observe the shape of the chamber signal. Unfortunately direct monitoring entails higher requirements in the matter of offset, noise and bandwith since the electronic must be able to follow the input.

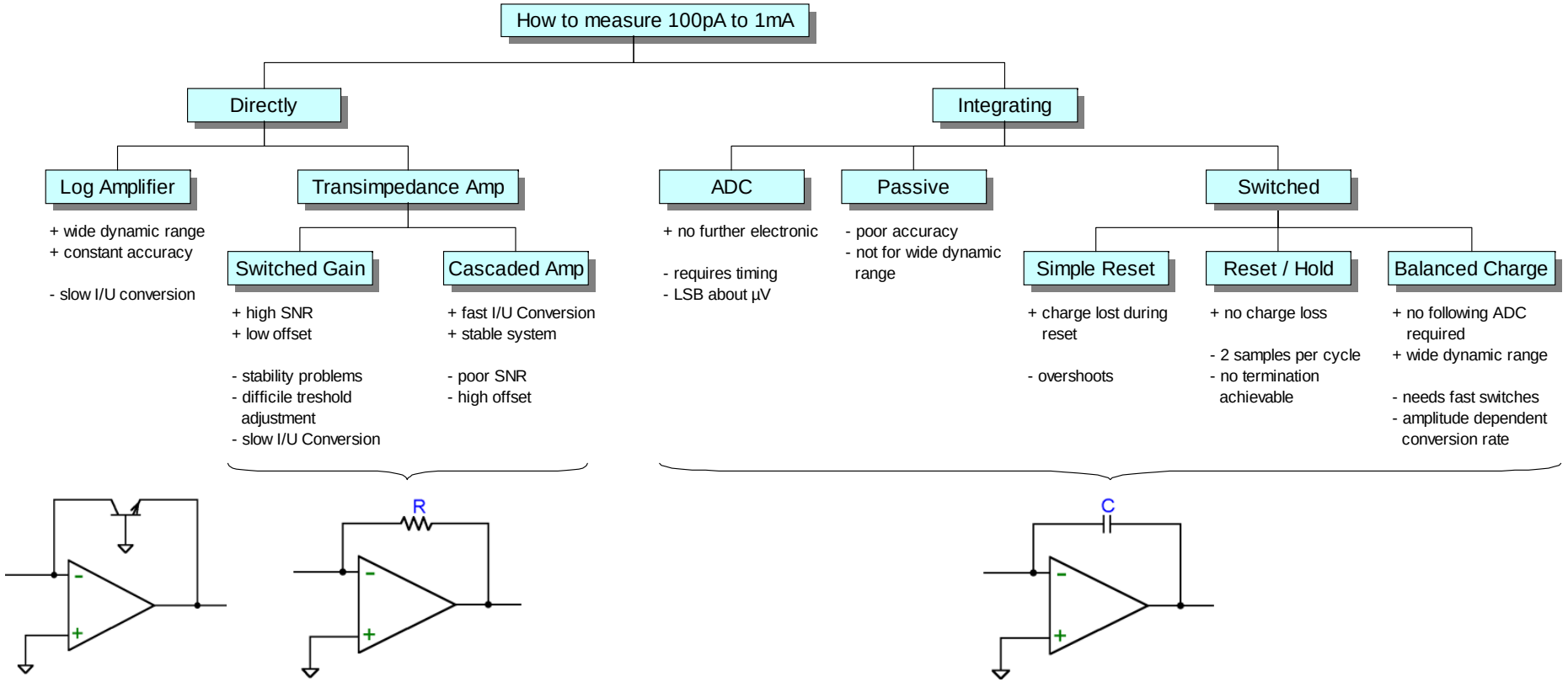


Figure 4 – Overview of the differerent possibilities to measure electric current

2.2.1 Logarithmic Amplifier

As shown in Figure 5, a logarithmic amplifier can be built up with an op amp and a bipolar transistor in the feedback loop. The circuit uses the exponential correlation between the collector current I_C and the base-emitter voltage U_{BE} at $U_{BC} = 0$ V.

$$I_C = I_{CS}(e^{\frac{U_{BE}}{U_T}} - 1) \tag{1}$$

Assuming an ideal op amp which draws no current, $I_e = I_C$ and $U_a = -U_{BE}$, we can write the output voltage as

$$U_a = -U_T \cdot \ln(\frac{I_e}{I_{CS}} + 1) \tag{2}$$

where $U_T = k \cdot T/e \approx 26$ mV at 25°C (k … Boltzmann constant, T … absolute temperature, e … electric charge). One can observe that the output is proportional to the logartihmus of the ratio between the input current and the collector reverse current. It should be emphasized that this circuit just illustrates the principle of a logarithmic amplifier. A more precise schematic can be taken from Burr Brown's Log100 datasheet or [3].

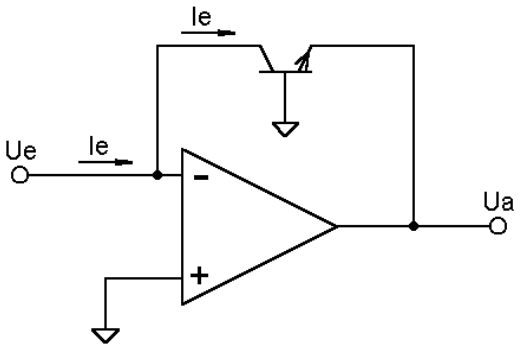


Figure 5 – Basic principle of a logarithmic amplifier

The properties of a logarithmic amplifier are

- a high dynamic range
- a constant accuracy over the whole measuring range

The disadvantage is

- a small bandwith which is also indirect proportional to the input current

2.2.2 Transimpedance Amplifier

A transimpedance amplifier is a circuit that converts an electric current into a proportional electric voltage. The principle is shown in Figure 6. Since the ratio between output and input is equal to a resistance, the gain of such an amplifier is specified in Ω.

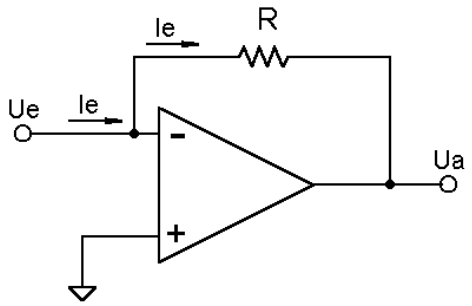


Figure 6 – Principle of a transimpedance amplifier

If we assume an ideal op amp, that draws no input current and has no offset voltage, the output voltage is

$$U_a = -R \cdot I_e \tag{3}$$

Unlike the logarithmic amplifier described above, the transimpedance amplifier provides an output voltage linear proportional to the input current. The advantage of this behavior is a constant linearity error over the whole dynamic range.

Unfortunately we have to amplify currents in the sub nA region. Assuming a 10 kΩ feedback resistor which converts 1 mA into 10 V, we have to deal with output voltages of 1 μV at the lower end of our input range. One can understand that this is not feasible with a single amplifier, if we predict a minimum offset of 10 μV and a rms noise voltage of at least the same value. Therefore we need to implement several gains for the different input ranges as you will see in chapter 3.2.3.

2.3 Integrating Monitoring Techniques

Unlike the direct monitoring the integrating techniques provide an average value over a certain time period. The drawback of getting an average current instead of an online display opposes less sensitivity to noise because of the reduced bandwith. Figure 7 shows the principle of an inverting integrator. If we take again an ideal op amp with no input current and offset voltage, we can calculate the output voltage U_a as

$$U_a = -\frac{1}{C}\int i_e(t)dt + U_{a0} \; . \tag{4}$$

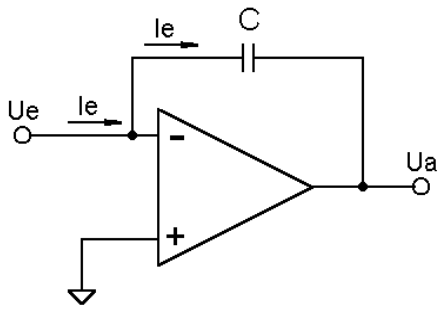


Figure 7 – Principle of an inverting integrator

All integrators, except for the passive version, have in common that they need to be reset after a particular time, otherwise the output would saturate. In other terms, the integration capacitor has to be discharged regularly. There are two basic principles how to do this. One possibility is to shorten the capacitor pins with a switch such as a FET, while another way is to discharge the capacitor with an induced current. Both options have its merits.

Shortening the integration capacitor is the simplest way to reset. A FET in parallel provides a convenient way to implement an analog switch. With the FET switched “on” its low drain-source resistance enables a fast discharge, while the high “off”-resistance assures an accurate signal integration. The tradeoff to the simplicity is the lost charge while resetting. In that case the signal current flows through the FET resistance instead of the integration capacitor.

This drawback is avoided if we induce a reference current of the opposed sign into the summing point of the op amp. As long as this current is higher than the maximum input current, the resulting current through the capacitor will lead to an opposed voltage change than with the signal current alone. The big advantage of this technique is that no charge is lost. The signal current will be integrated continously.

There are lots of Analog-to-Digital converters on the market which offer a current input. Unfortunately, we could not find an ADC which satisfies our specifications. Although some offer a very high dynamic range, the need of converting picoampere could neither fulfill. So we decided to use the principle but to accomplish a discrete design.

To summarize the advantages of integrating measuring techniques we can note

- high dynamic range

- low noise

The disadvantage is

- low bandwith
- no online display of the particle loss rate

2.4 Results

After weighing the pros and cons of each principle we decided to make further examinations in four circuits

1. Switched gain transimpedance amplifier
2. Transimpedance Amplifier with cascaded stages
3. Switched Integrator
4. Charge Balanced Integrator

We had to eliminate the logarithmic amplifier because of its high price and long delivery time. The specifications of different vendors showed also a poor bandwith. A market survey revealed that there are no ADCs with the required specifications available. Using a passive integrator doesn't work in our case because we don't have a sufficient long phase with no particles in the beam cycle. This time would be necessary to allow a discharge of the integration capacitor. The option with the reset/hold integrator has several interesting aspects but finally the fact that we can't terminate the input cable properly let us drop this solution.

3 Development of the Prototypes

3.1 Component modelling

To optimize the design process we used PSpice to simulate the different circuits before creating breadboard circuits. Unfortunately, not every component is covered in a Spice library so we had to create proper models in such a case.

3.1.1 The model of the chamber

According to chapter 1.2.2 we define the ionization chamber as an electric current source. Figure 8 shows the Norton equivalent of the circuit.

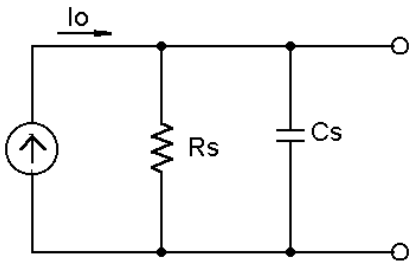


Figure 8 – Model of the chamber with parallel resistance and detector capacity

Since the ionization chamber doesn't consitute an ideal current source, we should add a parallel resistor R_S. However, preliminary measurements yielded to an output resistance of more than 10 GΩ, therefore we could neglect this resistor in our simulation. A much more serious property of the chamber is its capacity C_S. Measurements showed a value of about 100 pF. This high capacity degrades the phase margin of our electronic as we will see.

3.1.2 The model of the cable

The connection between the the ionization chamber and the analog front-end electronic is done by a 50 Ω coaxial cable. Its length vary between 10 m and 400 m. This is because of the different radiation exposure in the tunnel. The maximum dose for our front-end electronic is 10 Gy[3] per year. In the 4 arcs of the LHC this value will not be exceeded and therefore the distance between the ionization chamber and the front-end can be made as short as possible. A cable length of 10 m is predicted for these connections. Unfortunately, the radiation dose in the straight sections amounts to 40 Gy per year. Therefore the front-end has to be placed at the very end of the straight section resulting in a maximum cable length of 400 m.

To model the cable in Spice we used the ideal 'Transmission Line' as shown in Figure 9. The parameters are the characteristic impedance which is 50 Ω and the delay time which equals 5 μs/km. It should be mentioned that this assumption doesn't include the losses of the cable such as attenuation and dispersion. However, since we terminate the cable with its characteristic impedance we assume no reflections and a negligible DC attenuation because of the high impedance source. Nevertheless, further investigations have to be made on that issue.

[3] Unit for the exposure of radiation, 1 Gy = 1 J/kg

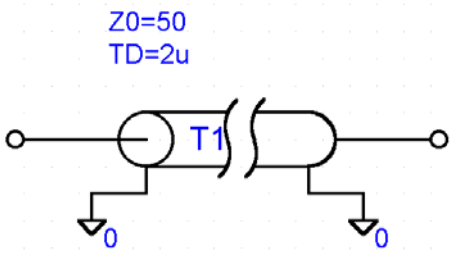


Figure 9 –Transmission line model of 400 m cable

3.2 Circuit Design

After chosing the suited principles we built up prototype circuits. The most helpful tool – aside skilled engineers and supervisors – was the circuit simulation with PSpice. First we created a simple model with many ideal assumptions. Then the schematic was refined until it represented the real circuit as good as possible. In the next step we created a breadboard circuit to test the functionality of the electronic. Since it is not practicable to make serious test series with breadboard ciruits (ground bouncing, interference) finally a soldered board was produced.

3.2.1 General design considerations

Low currents and high resistors

We got the task to monitor electric current from 100 pA to 1 mA. Whenever dealing with low currents and high impedance sensors one must be obvious of the parasitic effects, such as leakage currents. A high impedance sensor has the advantadge that it keeps the attenuation on the sensor cable small as long as it has to supply a low impedance load. It also reduces the effect of offset voltages of op amps, since the offset voltage generates only a small offset current through the source resistance.

On the other hand, extrem attention must be paid to a clean layout. If we want to use the high input resistance of an op amp, any leakage current over parasitic cable conductance or board traces must be avoided. It should be also noticed that in a case of a low current measurement we need an op amp with negligible input current. Otherwise, any bias current of the op amp will easily be added to the signal current.

Signal source

To create this signal current we used a precise voltage source in combination with a series resistor because no current source was available. The maximum voltage of this source was

10 V. Hence we used resistors from 10 kΩ, for creating mA, up to 100 MΩ and even 1 GΩ, to get pA. The same precautions as described above must be taken; that means, keep the resistor clean and dry and don't touch it during the measurment.

As described in section 3.1.2, we have to deal with a maximum cable length of 400 m at the input. For a proper examination of the circuit's performance this cable must be used for laboratory experiments. Unfortunately, we didn't have such a long coaxial cable in our laboratory. So we took a coil of 200 m multiwire, twisted pair cable and connected the wires in loops in order to create the desired length. In that case one must consider the different characteristic impedance of a twisted pair cable compared to a coaxial cable.

General Beam Loss considerations

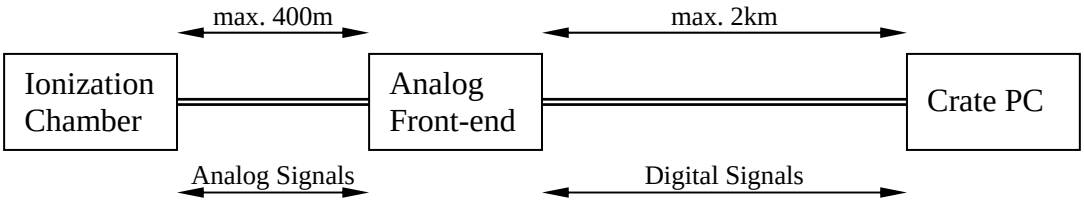
Another important fact is the overall number of beam loss monitors of 3000. This results in the need of a plug and play electronic. Therefore, any manual calibration like trimmers should be avoided.

It is also important to know the data treatment after the analog front-end since it will have a strong impact on the design.

Figure 10 shows the principle of our measurement chain. Because of the radiation, the signal condition has to be installed outside of the tunnel. This approach leads to a distance up to 2 km between the front-end and the crate, where the chamber signal finally is evaluated.

Figure 10 – The measurement chain of the Beam Loss Monitors

The following chapters show the results of the simulation as well as the results of the test



series in the laboratory. I want to mention that the different circuits are ordered chronologically.

3.2.2 Switched Integrator

I have to emphasize that even before we discussed the specifications and considered measurement principles I received a general introduction in accelerator physics as well as in beam loss monitors. The first was done by several lectures at the CERN summer school while the latter had been accomplished by testing and analyzing the circuit in Figure 11. It shows a switched integrator circuit as described in [2]. This circuit portrays one of the first proposals for the beam loss front-end.

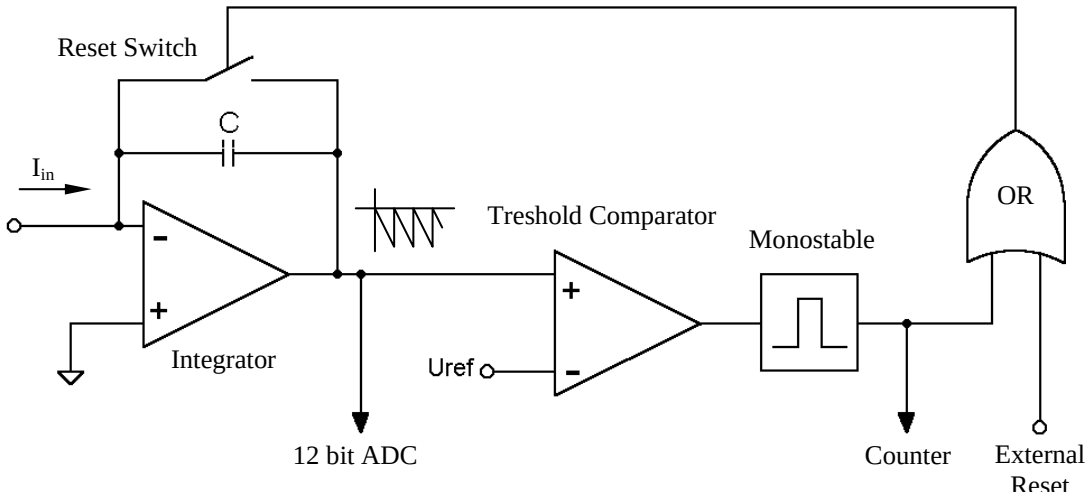


Figure 11 – Switched Integrator with Reset

It consitsts of a regularly reset integrator with an integration time of 20 ms [4]. If one applies an electric current to the input of the op amp, it will be integrated. Let us assume a constant input signal, hence the output voltage of the integrator ramps either negative or positive depending on the inputs' sign. Our circuit is restricted to unipolar operation and we will get only a negative output voltage as indicated in the schematic. At the end of the integration period, the integrator output will be sampled with an ADC (this part hasn't been considered). Unfortunately, we can't cope the whole dynamic range only with that ADC. Assuming a maximum input voltage of -5 V, we would need an LSB of $-5/10^7 = 0.5\ \mu V$ corresponding to 23.3 effective bits. We didn't find an ADC on the market which such an high dynamic range.

To overcome the task a sophisticated approach was made. The ADC should be able to handle about 3 decades according to its number of bits, therefore a 12 bit ADC was suggested. In addition, the integrator was designed to provide the maximum of -5 V at 100 nA. If the

[4] Here the advantage of infinite power supply noise suppression is taken, since the integration period equals the line frequency period.

integrator output exceeds -5 V, the treshold comparator triggers a reset. So there are two reset conditions:

1. The integration time of 20 ms is reached.
2. The integrator output hits the treshold level of -5 V.

If the second case is true, a counter is incremented. When the last ramp finally reaches the 20 ms time period, the integerator is reset as well as this last voltage is converted to a digital number by the ADC. Hence the current is the sum of two values, the number stored in the counter and the number provided by the ADC.

Design Consideration

The detailed schematic is shown in Appendix A.

Integrator

The input impedance of the circuit should match the characteristic impedance of the sensor cable. According the cable manufacturer's specification the characteristic impedance equals 110 Ω. Therefore we used the same value for the input resistor to terminate the system properly.
For the integrator itself we used the Burr Brown ACF2101 because it has proven its performance in former projects at CERN. The most important parameters are

- Bias current I_b = 100 fA
- Slew Rate SR = 3 V/μs
- Offset Voltage $U_0 = \pm$ 10 μV

To use the maximum slew rate at 1 mA, we have to size the feedback capacitor as

$$C_{Int} = \frac{1mA}{3V/\mu s} = 333pF \tag{5}$$

Hence we connected 220 pF in parallel to the internal 100 pF capacitor of the ACF2101.

Threshold comparator

To trigger the internal reset we used a LM311 voltage comparator with its inverting input tied to -5V. Since the integrator output will immediately rise back to 0V after triggering a reset, we didn't include a hysteresis.

Reset pulse generator

We used a 74LS123 monoflop to create a 1 µs long reset pulse. This reset time is determined by the values of an external resistor and capacitor. The output signal is connected to a OR gate. So we reset either if we reach the 20 ms border or in case of a comparator trigger. Since you can't drive the FET for resetting with a TTL output we had to convert that level to a –10 V gate voltage which is sufficient to switch the FET. Therefore we used the AD7510DI analog switch.

Reset switch

The reset itself is accomplished by discharging the integration capacitor over the low "on" resistance of a FET. Although the chip inherits an own reset switch we were forced to use an external one since the internal switch uses a 1.5 kΩ resistor in series. This high value would extend the reset time to several microseconds.

For the FET switch, the IT1700 was used because of its outstanding C_{DS} and C_{GS} respectively. This leads to a small charge injection: The problem with resetting the integrator is that at every reset operation a certain charge is injected in the integration capacitor via the parasitic capacities of the FET. One can observe this charge injection in an offset step at the beginning of the ramp. The datasheet of the IT1700 claims an r_{DSon} of 75 Ω establishing a reset time of less than 1 µs. Finally it should be mentioned that the reset time doesn't only depend on the RC combination of the integration capacitor and r_{DSon} but on the finite bandwith of the op amp. This extends the reset time beyond 5·RC. With the cable connected to the input the circuit reacts even worse – if the reset impulse is too short, one will observe a certain overshoot due to the reduced phase margin with the cable.

Results

We performed both a PSpice simulation and laboratory test series. Figure 12 shows the output characteristic of the switched integrator. From 100 pA to 100 nA it works in pure ramping mode, generating a sampled value at the end of the 20 ms integration period. Above 100 nA the ACF2101 is reset by the comparator. Each reset increases the counter. To have a comparable number, the plot shows the measured charge per 20 ms as the output signal. One can observe that the curve bends dramatically at high currents. This is due to the 1 µs reset pulses which constitute almost half of the 20 ms period.

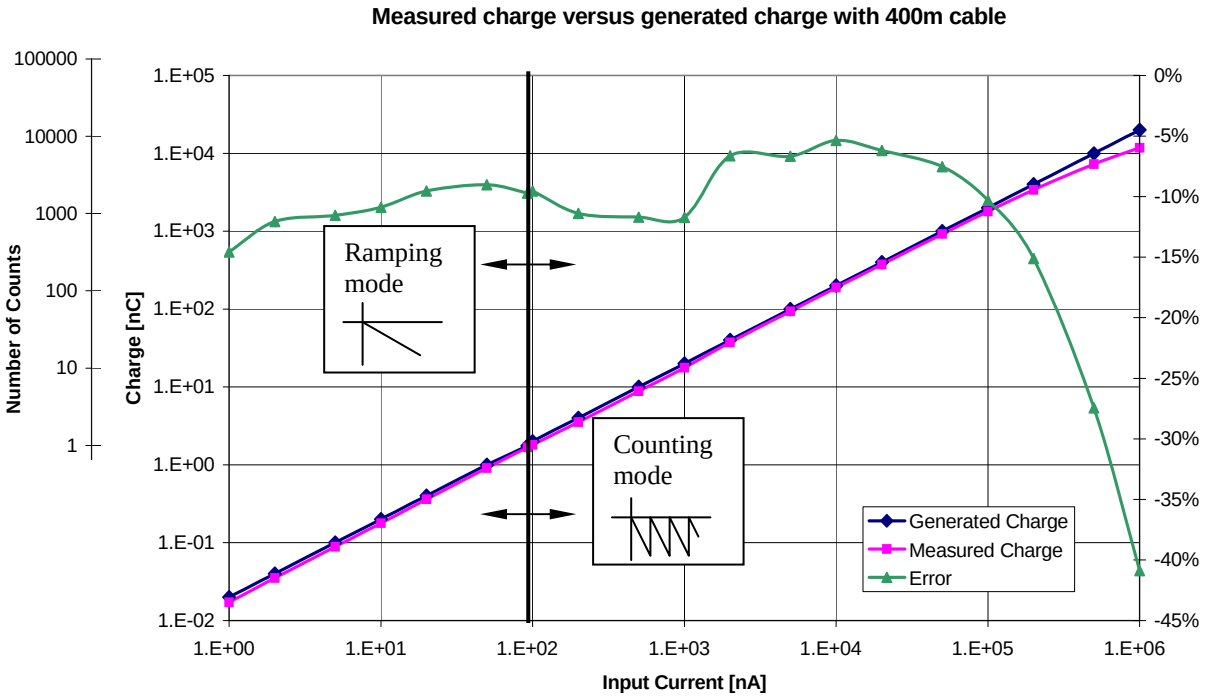


Figure 12 – Measured charge with the AFC2101 versus generated charge with 400m cable

Several simulations have been performed and compared with the measured integrator output. Figure 13 shows the recorded waveform in comparison to the simulation result at an input current of 0.20 µA. One can distinguish between the 20 ms external reset and the reset triggered by hitting the –5 V treshold.

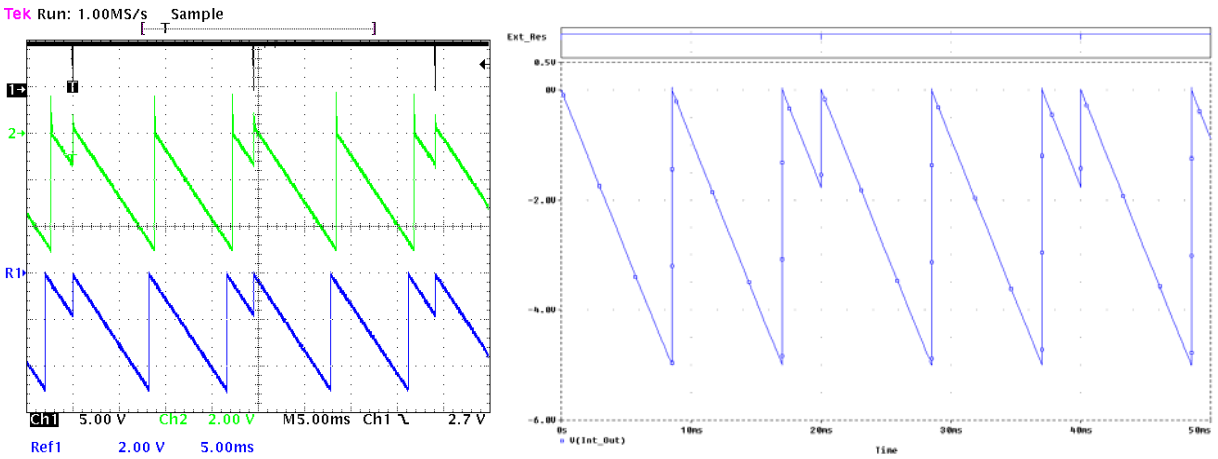


Figure 13 – Integrator output at 0.2 µA; the left picture shows the measured waveforms with the scope. The lower waveform is without and the middle with 400 m cable (recognize the overshoot). The signal on top indicates the external reset. The right picture illustrates the simulation results with PSpice without the cable.

3.2.3 Transimpedance Amplifier

The transimpedance amplifier is a linear current-to-voltage converter. Since we are not able to handle the whole 7 decades range we had to change the gain. There are two possibilities indicated in Figure 14 to achieve this and each has its merits:

1. Changing the feedback resistance
2. Switching a second high gain stage in series

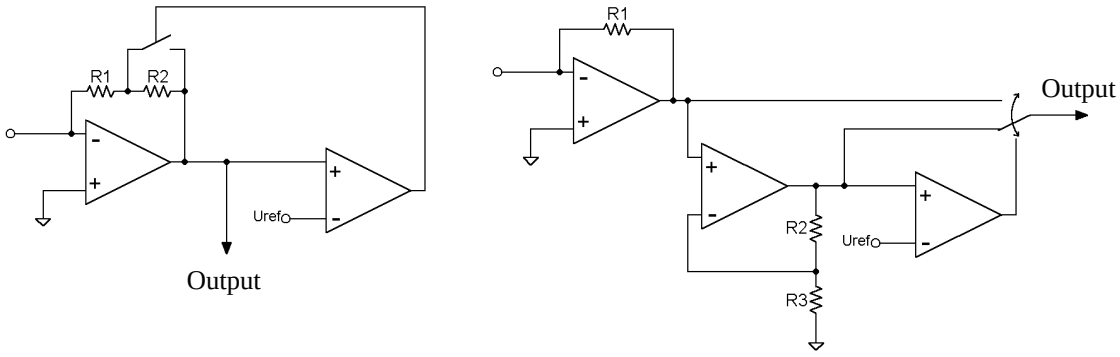


Figure 14 – Transimpedance Amplifier with switched gain (left) and with a second stage amplifier (right)

Ad 1)

First we tried to change the feedback resistor according to the output voltage as indicated in the left part of Figure 14. The detailed schematic is shown in Appendix B. We used two voltage comparators at the output to switch the gain. This was performed by shortening one of the resistors in the feedback with an analog switch. The control signal of the switch provides

the additional information which gain has actually been selected. Finally the amplifier's output is converted into a digital number equal to the loss rate of the ionization chamber.

Amplifier

To measure low currents, the right choice of the op amp is one of the most important decisions to be made. After comparing several op amps from different vendors we took the OPA627 from Burr Brown. Its properties are

- Bias Current $I_b = 2$ pA
- Offset Voltage $U_0 = 100\ \mu V$
- Gain Bandwith $f_T = 16$ MHz

As mentionied above, the maximum output voltage of the transimpedance amplifier was set to 10 V. The whole circuit is designed for a maximum current of 1 mA, therefore the feedback resistor yields to

$$R_1 = \frac{U_{out(\max)}}{I_{in(\max)}} = \frac{10V}{1mA} = 10\ k\Omega\,. \tag{6}$$

This resistor is used to measure high currents. At low input currents we increased the gain by a factor of 500 leading to a feedback resistor of (neglecting the 10 kΩ in series)

$$R_2 = 500 \cdot R_1 = 5\ M\Omega\,. \tag{7}$$

The next step was to compensate the capacity at the op amp input. This capacity is formed by the chamber and the cable respectively. If you calculate the feedback function of a transimpedance amplifier you will notice an increased phase shift due to this capacity. This phase shift leads to overshoots. Even worse, it could make the whole circuit oscillate since after triggering one comparator level the overshoot exceeds the other immediately and so on. Therefore capacitors in parallel to the feedback resistors are obliged. Circuit simulations and test series lead to 8.6 pF || 5 MΩ and 5.6 nF || 10 kΩ respectively[5]. To change the gain R2 and C2 are shortened with an AD7510DI analog switch.

[5] The reader is refered to Burr Brown application note for an exactly treatment of transimpedance amplifiers and its compensation.

Comparators

The gain is controlled with 2 voltage comparators. We took the LM311 for that task. We have to observe two tresholds according the maximum of each range. We chose the tresholds 10 V and 10 mV respectively. If one assumes a low current the circuit operates with high gain of 5 MΩ. If the losses increase we reach 10 V equal to 2 µA. Now the gain is changed to 10 kΩ lowering the output voltage to 20 mV. If the losses decrease again, we reach the lower treshold of 10 mV at 1µA. After the switching action the output goes to 5V. Therefore the hysteresis factor is 2.

The comparator signals are connected to a SR latch which controls the analog switch.

Results

It was not easy to get a stable circuit because of the input capacity. Therefore we used a certain hysteresis between the two gains as well as compensation capacitors in parallel to the feedback resistors. Unfortunately, this reduces the bandwith. Although the circuit worked now stable we gave up that solution and produced no soldered protoype.

Figure 15 shows the results with the breadboard circuit. We applied a triangle wave with an amplitude of 4 µA and a period of 10 ms. The left picture was made with proper phase compensation while the right one indicates oscillation with 400 m cable at the input. To get a stable signal we adjusted the lower treshold as indiciated in the lower waveform. Figure 16 shows the waveforms of the PSpice simulation.

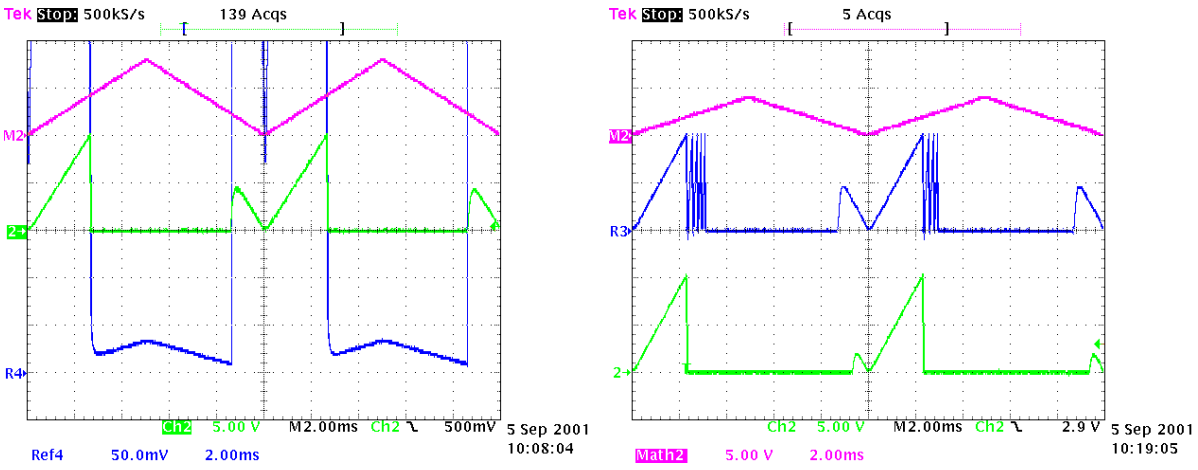


Figure 15 – Output signals of the transimpedance amplifier with switched gain at 4 µA triangle input current. Left picture: Proper phase compensation, Ch2 is the output signal while R4 magnifies the sector with low gain. Right picure: Same input signal but with 400 m cable at the input (R3) and adjusted tresholds for stable operation (Ch2).

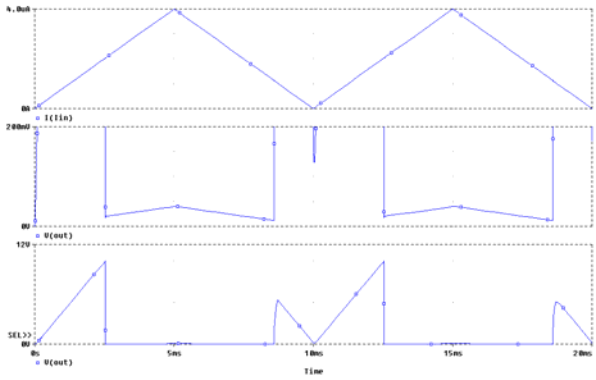


Figure 16 – PSpice simulation of Figure 15

Ad 2)

The other possibility to change the gain is the usage of two cascaded amplifier stages as illustrated in the right half of Figure 14, the detailed schematic can be found in Appendix C. The circuit consists of a transimpedance amplifier plus a following noninverting amplifier. The transimpedance amplifier converts the signal current into a voltage. In the case of high losses (= high current) this voltage can be sampled directly. If we have to sense low currents, the output voltage of the transimpedance amplifier is too small for reliable acquisition. Therefore we amplify this small voltage by a factor 1000 to get appropriate values.

However, this second stage does not only amplify the signal but also the noise and the offset of the former stage – not forgetting to add also the second stage's noise plus offset. So we need an amplifier with low offset voltage and noise for this task. Nevertheless, even the best op amp can't resolve this problem satisfying. So we reduced the noise by decreasing the bandwith of the amplifier with a capacitor in parallel to R5. Unfortunately the offset error still remains.

To decide which amplifier output will be transmitted, we used a comparator to surveille the second stage's voltage. If this voltage exceeds 10 V then the transimpedance output is transmitted otherwise the second stage. This multiplexing is accomplished by an analog switch.

Input Amplifier

We based the design on the former transimpedance solution with switched gain. The feedback resistor was reduced to a single 10 kΩ resistor and the OPA627 still remained due to its

remarkable properties. One should notice that we didn't need a capacitor parallel to the feedback resistor anymore. According to (6) we get 10 V at 1 mA maximum input current.

Second Stage

To observe the low losses we amplified the output of the first stage by 1000. Hence we get an output of 10 V equal to 1 μA. A 100 pF capacitor was switched in parallel to R5 to form a low pass. This should reduce the bandwith and therefore the noise.

Comparator

In contrast to the switched gain amplifer we only observe the output of the second stage. A simple voltage comparator, again the LM311, was used. The tresholds equal 10 V for rising signals and 5 V for falling signals, according to 1 μA and 500 nA input current.

Analog Multiplexer

The comparator output controls a AD7512DI analog switch. Hence depending on the comparator signal either the first or the second stage is switched to a following ADC.

Results

The advantage of this solution is the higher reliability since no oscillation can occur. The bandwith is limited only for small currents. Unfortunately, the generated offset and noise is much higher than in the pure transimpedance circuit. It should be noticed that trimming the offset is a quite difficult task since the high gain of the second stage makes the output very sensitive to minor changes. Furthermore, no offset trimmers should be implemented in the final circuit. Thus the output of the second stage can also show negative voltages. This implicates the necessary of a bipolar ADC for the signal conversion.

Figure 17 shows the result of a test series. The signal was measured from 1 mA down to 100 pA and vice versa to indicate the hysteresis. The high offset of 100 mV should be recognized. Even with an offset corrected value high linearity errors occured. Figure 18 illustrates the output with the same input signal as in Figure 15.

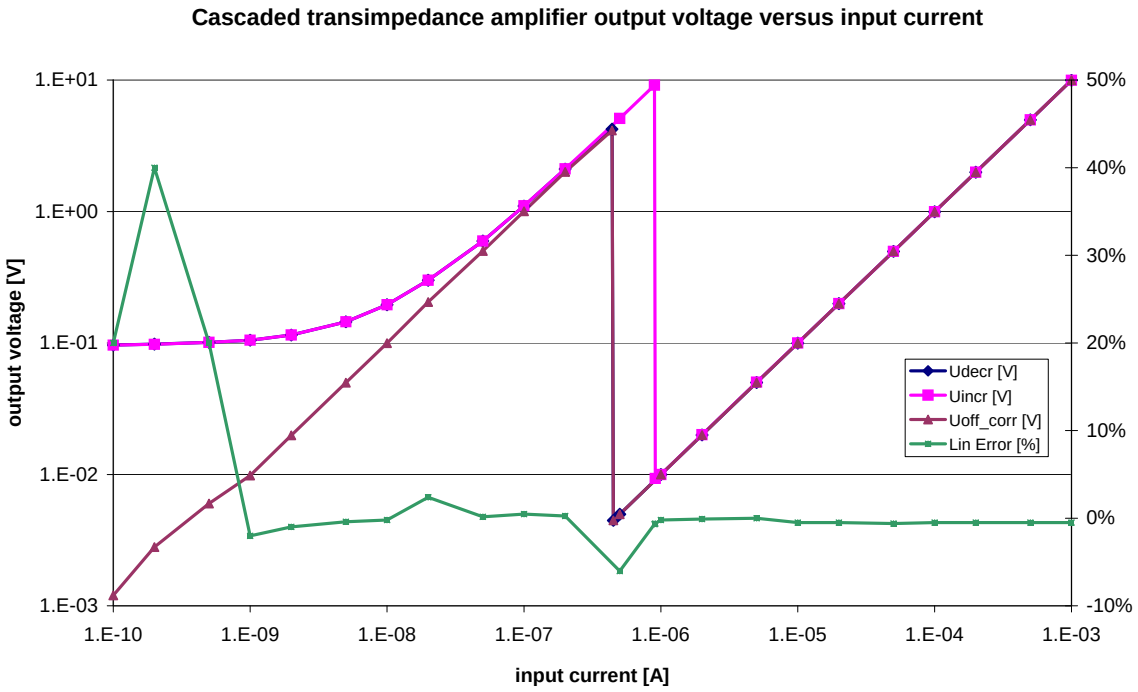


Figure 17 – Output voltage of the cascaded transimpedance amplifier with 400 m input cable

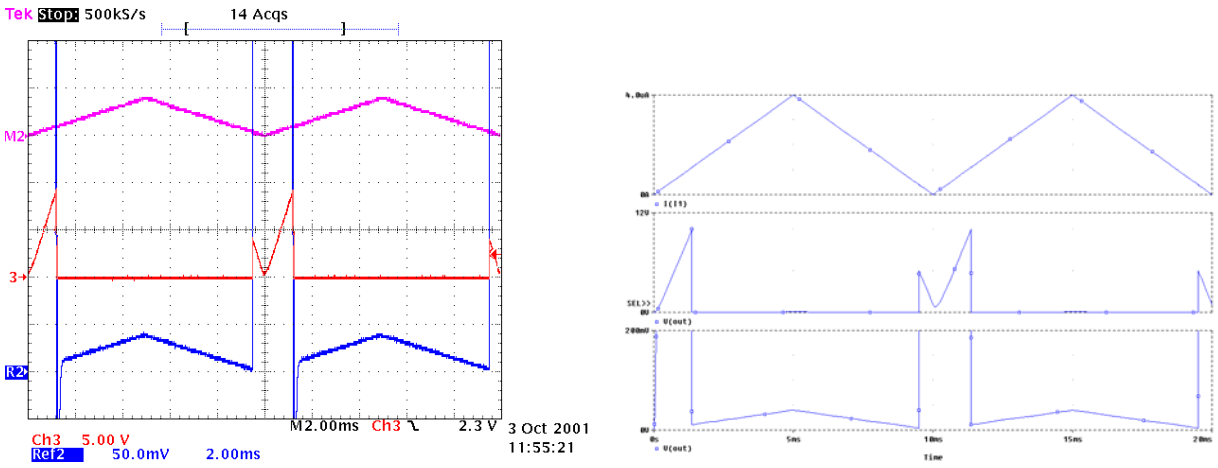


Figure 18 – Measured waveform (left) and simulation results (rigth) with the same conditions as in ….

3.2.4 Current-to-Frequency Converter

After examining direct monitoring techniques we went back to an integral solution. The question we don't have to forget is how to transmit the front-end output to the dump controller. Because of the radiation in the tunnel, this controller has to be placed on the surface leading to a certain distance to the front-end circuit. According to 3.2.1 this distance will be about 1 to 2 km.

For sure we can't transmit analog voltages over this distance since the attenuation will lead to inaccurate results. So it has to be a digital signal or at least a kind of discrete signal.

Therefore the idea came up to convert the voltage respective the current into a frequency to transmit it over the long cable. We tried the VFC110 from Burr Brown and searched on the Web for different voltage-to-frequency converters but none of the devices could fulfill our specifications. So we decided to build up a converter with discrete components according to our problem. At this point I have to mention the useful discussions with my FH supervisor.

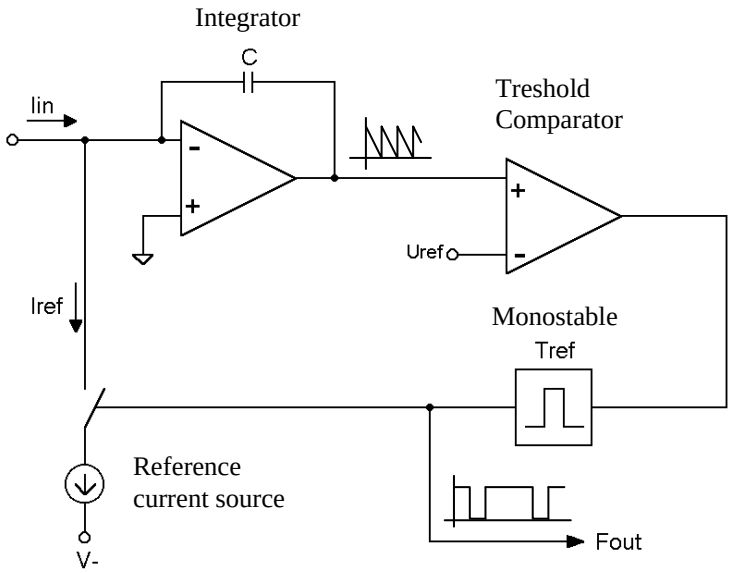


Figure 19 – Principle of the charged balanced current-to-frequency converter

Figure 19 shows the basic principle of the current-to-frequency converter (CFC). It works on the principle of balanced charge and consists of an integrator which is reset by inducing a fixed reference current. If we assume a positive input current, the output voltage ramps negative. After hitting a treshold, the reference current is connected to the summing node for a fixed time interval ΔT. Since the reference current flows in the opposite direction than the signal current, the integrator output is driven back. The output frequency is proportional to the input current and can be calculated as

$$f_{out} = \frac{\frac{1}{T}\int_{T} i_{in}\,dt}{I_{ref} \cdot \Delta T} \tag{8}$$

where T equals the period of f_{out}.

Design Consideration

The final version of this circuit is shown in Appendix D. After developing a PSpice simulation with we started to optimze the design. There are several points which are important. First, one will see from Equation (8) that the integration capacitor doesn't occur. Thus the output frequency is independent of its exact value. Nevertheless it should be mentioned that the capacitor sets the amplitude of the integrator. This is important considering the dynamic behavior of the circuit. A small capacitor value leads to a bigger du_a/dt. This can lead to problems with the correct termination of the cable impedance since the inverting node could not be held exactly at 0 V mainly due to the op amp's finite bandwith.

Integrator

We used the well known OPA627 with a 1 nF capacitor in the feedback. This value gives a voltage rise of 1 V/μs at the maximum input current of 1 mA. To terminate the input cable properly we took a 50 Ω resistor. One will recognize the capacitor at the inverting input. It is used to store fast pulses and transmit the accumulated charge "slowly" to the integrator. This is a standard procedure for detector readout electronics in high energy physics.

Comparator

First we tried again with the LM311 but experiments showed that its propagation time of 200 ns is too high. Hence we replaced it by the NE521. This comparator has a propagation time of only 4 ns but needs a ±5 V supply.

Monostable

There are different possibilities to create a short pulse. We took a 74HCT123 monostable and adjusted the reference time to ΔT = 500 ns. This yields to a frequency of 1 MHz at 1 mA input current. We also tried a TLC555 precision timer, but tests revealed that it couldn't generate such a short pulse.

Reference Current source

To create I_{ref} a simple transistor current source has been designed. The tests with this circuit yield to a sufficient accuracy and stability, so we didn't consider using an op amp current source. Anyway, it isn't yet desided how many front-end channels will be placed on one

board. For several channels we could think about one precise reference source and current mirrors to distribute the current to each channel.

Current switch

We tried different switches such as diodes, N- and P-channel JFETs. Finally we agreed on using a series-shunt switch with J176 P-channel JFETs. This has the advantage that we can drive the JFETs directly with the monostable output. N-channel JFETs are faster and have less r_{DSon} but they need a negative gate voltage.

Results

The CFC showed good linearity and accuracy over the whole dynamic range as illustrated in Figure 20. The maximum error from 100 pA to 1 mA is –0.8%. One can clearly observe the change of the series resistor of our signal source. Therefore, we expect even better results with a current source, such as an ionization chamber. The cirucit provides an acquisition time of 1 µs at 1 mA and 1 s at 1 nA respectively. Since we don't need fast sampling at low currents this porperty doesn't mean a disadvantage.

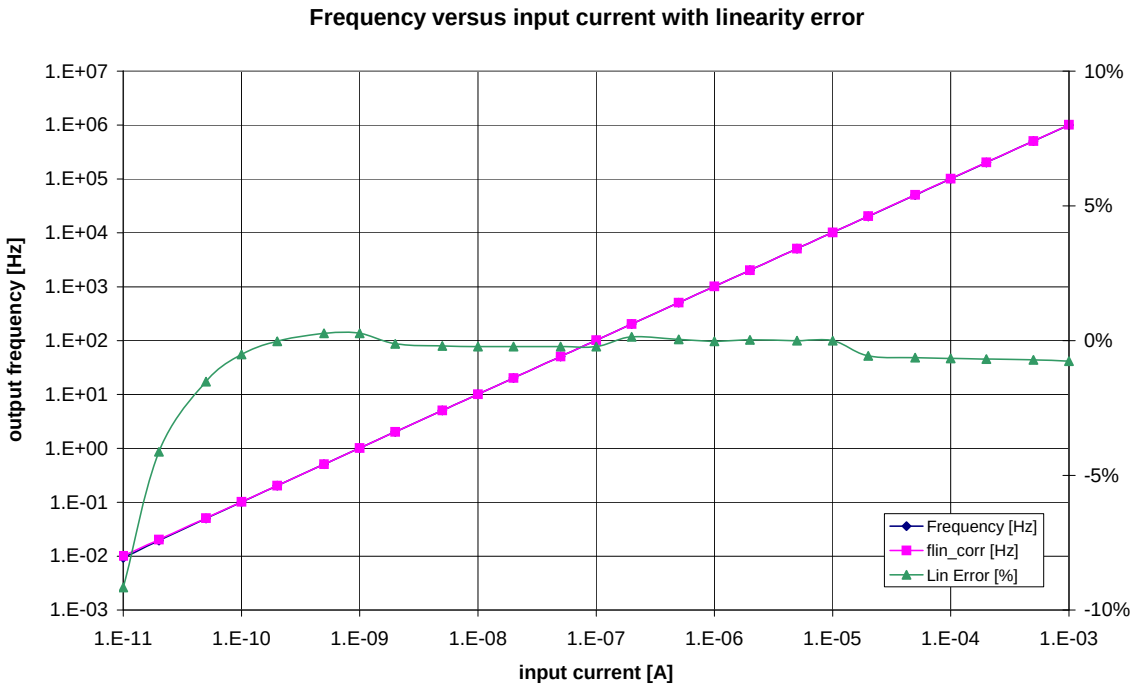


Figure 20 – Output frequency of the CFC versus input current with linearity error

Before creating a test board, PSpice simulations have been performed. Figure 21 shows the integrator and monostable output at a current of 1 mA in comparison to the measured signals with the scope. Both pictures take 400 m cable at the input into account.

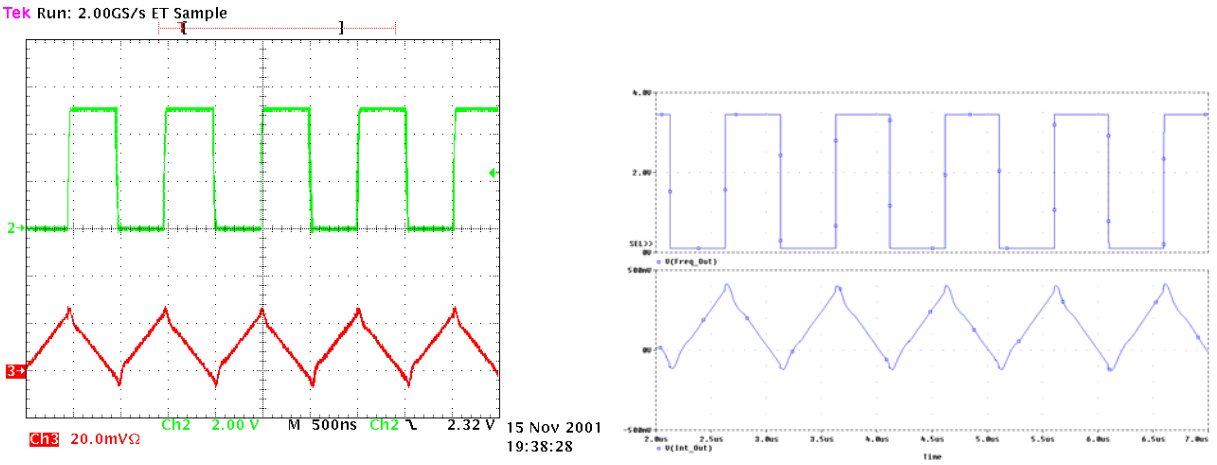


Figure 21 – CFC at 1 mA signal current and 400 m cable; integrator output (lower waveform) and monostable output (upper waveform). The left picture shows the measured waveforms while the right one illustrates the simulated signals

4 Summary

The beam loss system of the LHC makes high demands in terms of dynamic range, wiring issues and a free calibrating analog front-end electronic. The long cabling distance between the front-end place and the beam dump controller because of radiation exposure states another strong impact on the overall design considerations. To overcame this task different measurement techniques have been examined in order to determine their capability to handle all the required specifications. Several circuits have been simulated as well as investigated in the laboratory.

The switched integrator with reset is not favored because of the lost charge in the reset operations which produces too much error. Another approach has been a transimpedance amplifier with switched gain. The circuit has critical properties in terms of stability and bandwith, therefore we excluded this solution for further investigations. Measuring the loss rate with a two stage amplifier overcomes the stability problem but creates much noise and offset voltage. A digital offset compensation seems inescapable. Nevertheless, the basic

concept constitutes a well known solution for beam loss monitors (DAISY[6], RHIC[7], SPS) – of course with much less dynamic range.

From the present point of view the current-to-frequency converter seems to be the most appropriate solution. It doesn't need a digital offset correction, it delivers an averaged value of the particle loss rate which means low noise as well as no further digital integration and it could measure over a dynamic range of 160 dB without changing the feedback capacitor. However the design is not optimzed and futher investigation will be made.

[6] Deutsches Elektronen Synchrotron, Hamburg, Germany
[7] Relativistic Heavy Ion Colldider, Brookhaven Institute, USA

5 List of Abbreviations

ADC	Analog-to-digital converter
LHC	Large Hadron Collider
CFC	Current-to-Frequency converter
op amp	operational amplifier

6 Table of Figures

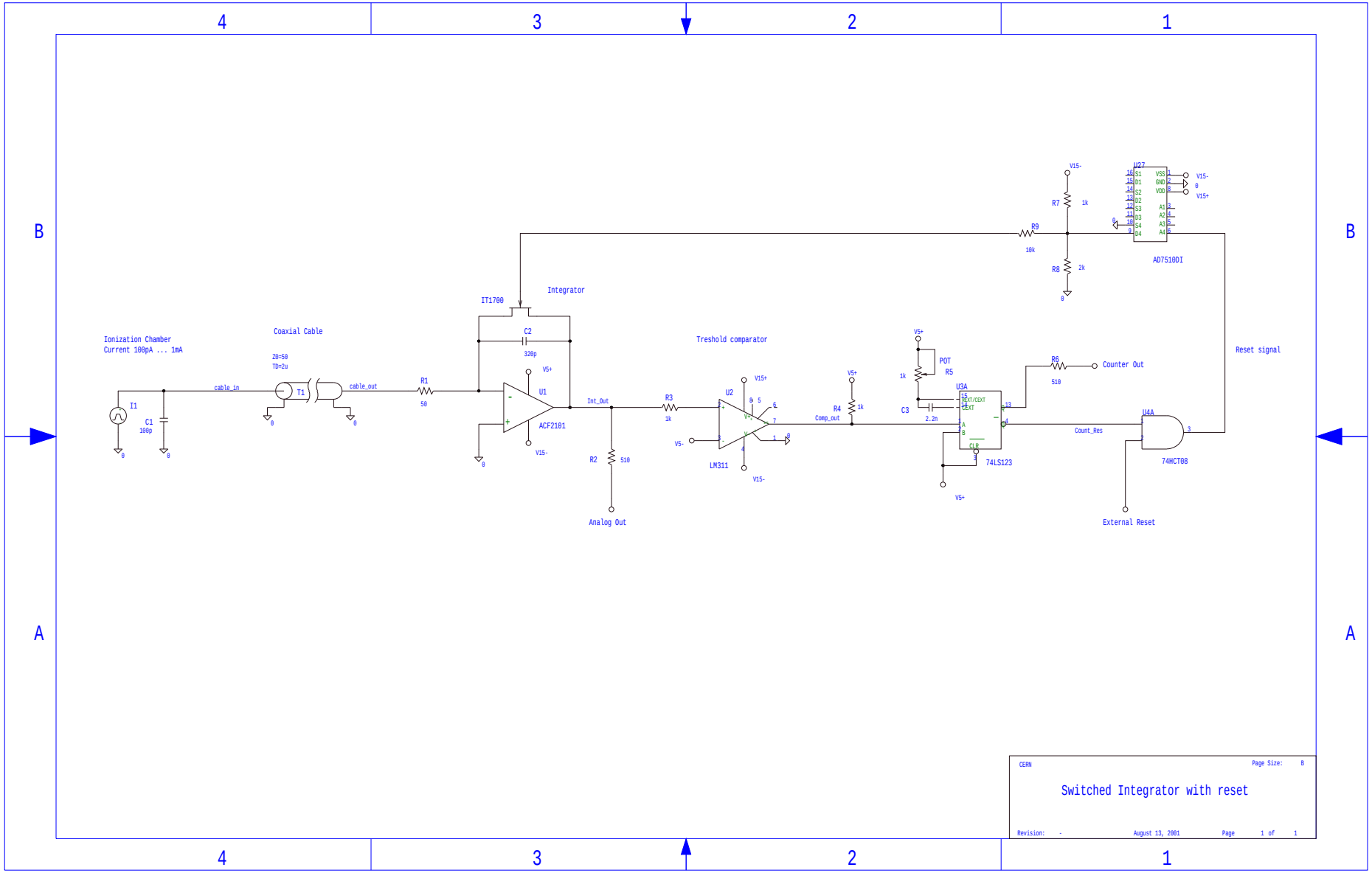
7 Bibliography

[1] Communications & Public Education Group, CERN the international leading laboratory for particle physics, Information leaflet, October 1998

[2] E. Gschwendtner et al., LHC Beam Loss Monitors, SL Note 01-27, CERN, (2001)

[3] P. Horowitz, W. Hill, Die Hohe Schule der Elektronik, Elektor 1980, p. 245 – 250

8 Appendix


4
3
2
1
B
A
Ionization Chamber
Current 100pA ... 1mA
I1
C1
100p
cable_in
Coaxial Cable
Z0=50
TD=2u
T1
cable_out
R1
50
IT1700
Integrator
C2
320p
U1
ACF2101
V5+
V15-
Int_Out
R2
510
Analog Out
R3
1k
Treshold comparator
U2
LM311
V5-
R4
1k
Comp_out
POT
R5
1k
C3
2.2n
U3A
74LS123
R6
510
Counter Out
Count_Res
U4A
74HCT08
External Reset
R7
1k
R8
2k
R9
10k
U27
AD7510DI
Reset signal
CERN
Page Size: B
Switched Integrator with reset
Revision: -
August 13, 2001
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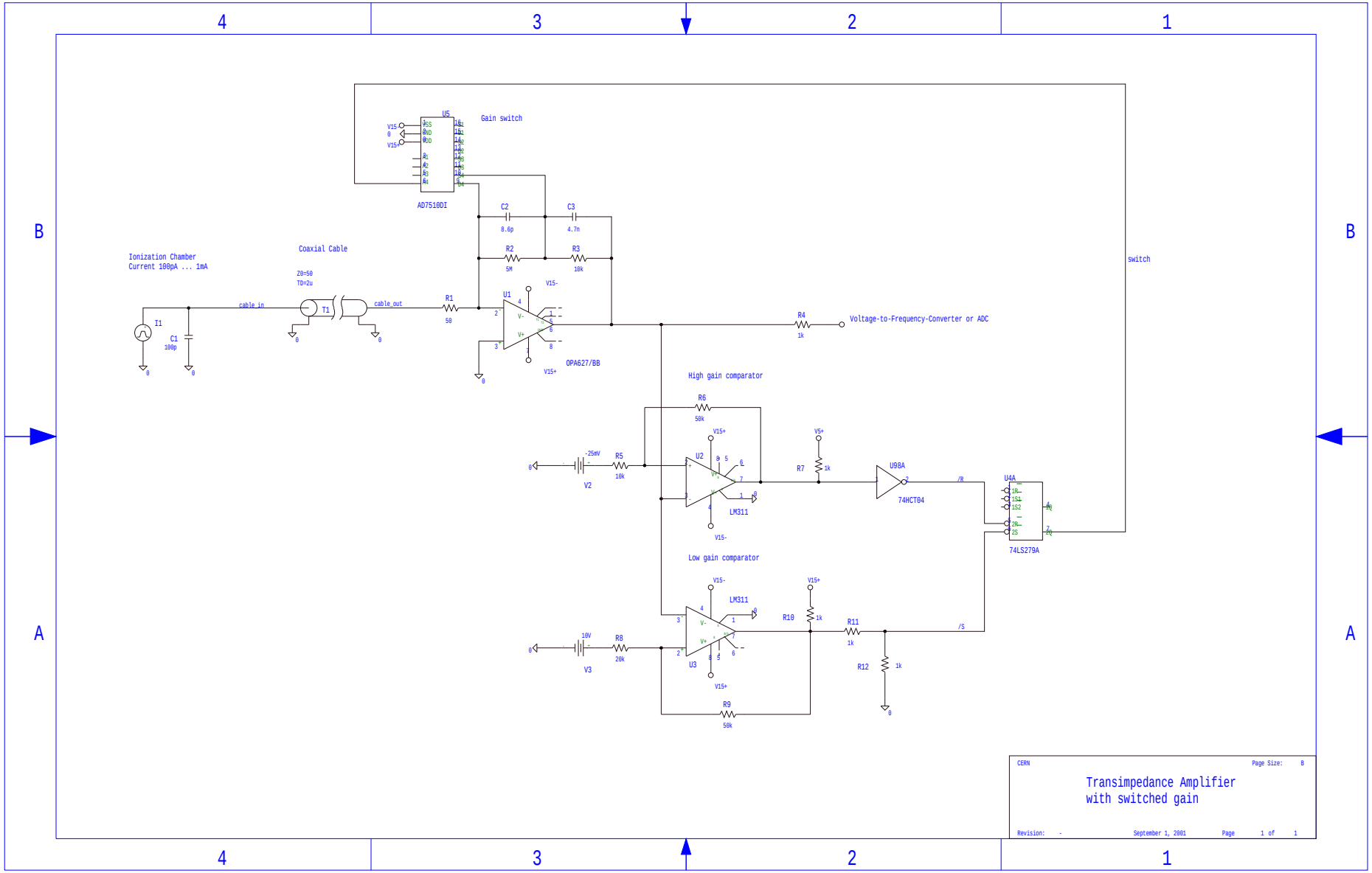
Gain switch
U5
AD7510DI
C2
8.6p
C3
4.7n
R2
5M
R3
10k
switch
Ionization Chamber
Current 100pA ... 1mA
Coaxial Cable
Z0=50
TD=2u
cable_in
cable_out
T1
I1
C1
100p
R1
50
U1
OPA627/BB
V15-
V15+
R4
1k
Voltage-to-Frequency-Converter or ADC
High gain comparator
R6
50k
-25mV
V2
R5
10k
U2
LM311
R7
1k
U98A
74HCT04
/R
U4A
74LS279A
Low gain comparator
10V
V3
R8
20k
U3
LM311
R10
1k
R11
1k
/S
R12
1k
R9
50k
CERN
Page Size: B
Transimpedance Amplifier
with Switched gain
Revision: -
September 1, 2001
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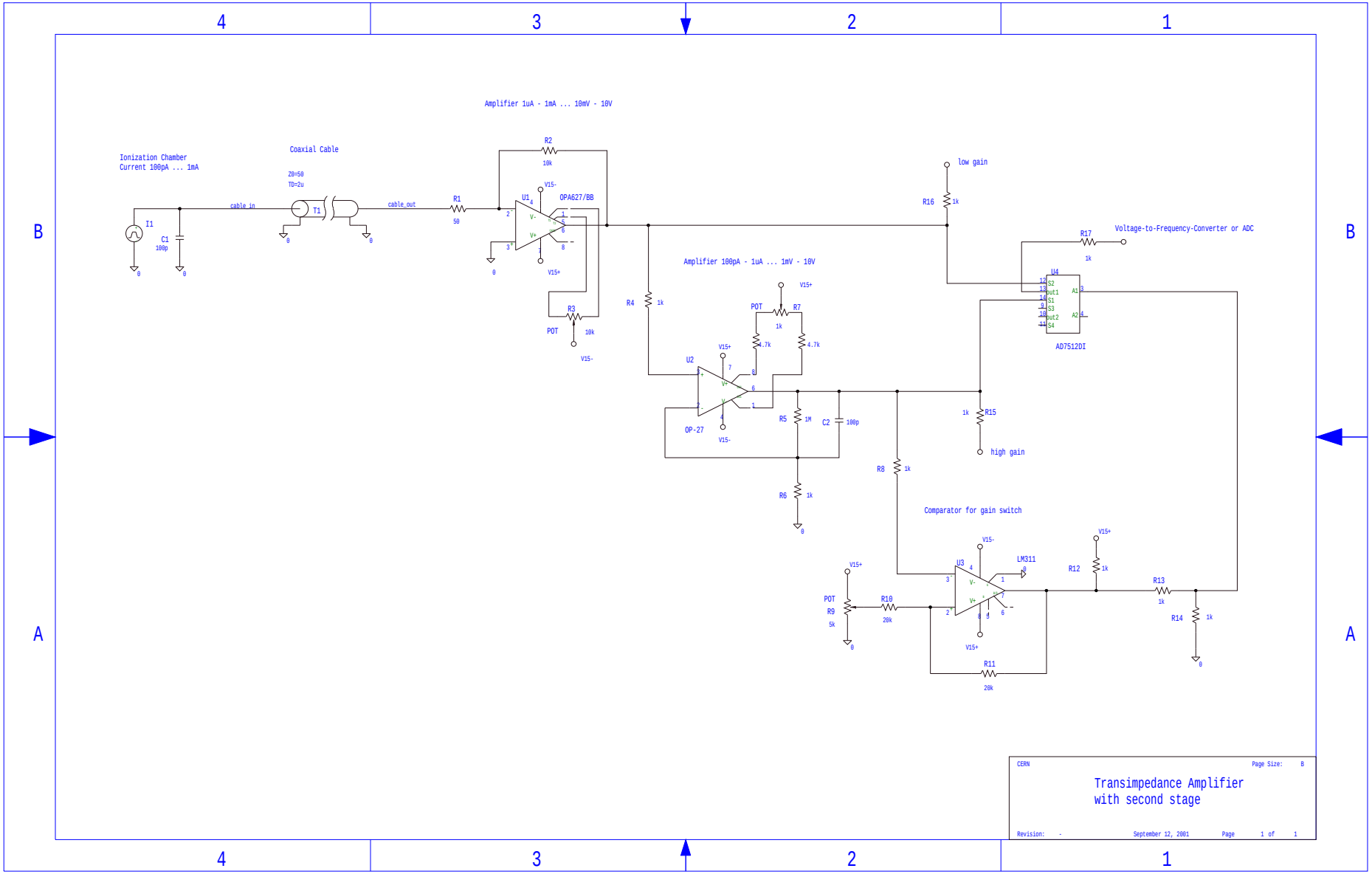
4
3
2
1
B
A
Amplifier 1uA - 1mA ... 10mV - 10V
Ionization Chamber
Current 100pA ... 1mA
Coaxial Cable
Z0=50
TD=2u
cable_in
cable_out
I1
C1
100p
T1
R1
50
R2
10k
U1
OPA627/BB
V15-
V15+
R3
POT
10k
low gain
R16
1k
Amplifier 100pA - 1uA ... 1mV - 10V
R4
1k
POT
R7
1k
4.7k
4.7k
U2
OP-27
R5
1M
C2
100p
R6
1k
R8
1k
1k
R15
high gain
Voltage-to-Frequency-Converter or ADC
R17
1k
U4
AD7512DI
Comparator for gain switch
U3
LM311
POT
R9
5k
R10
20k
R11
20k
R12
1k
R13
1k
R14
1k
CERN
Page Size: B
Transimpedance Amplifier
with second stage
Revision: -
September 12, 2001
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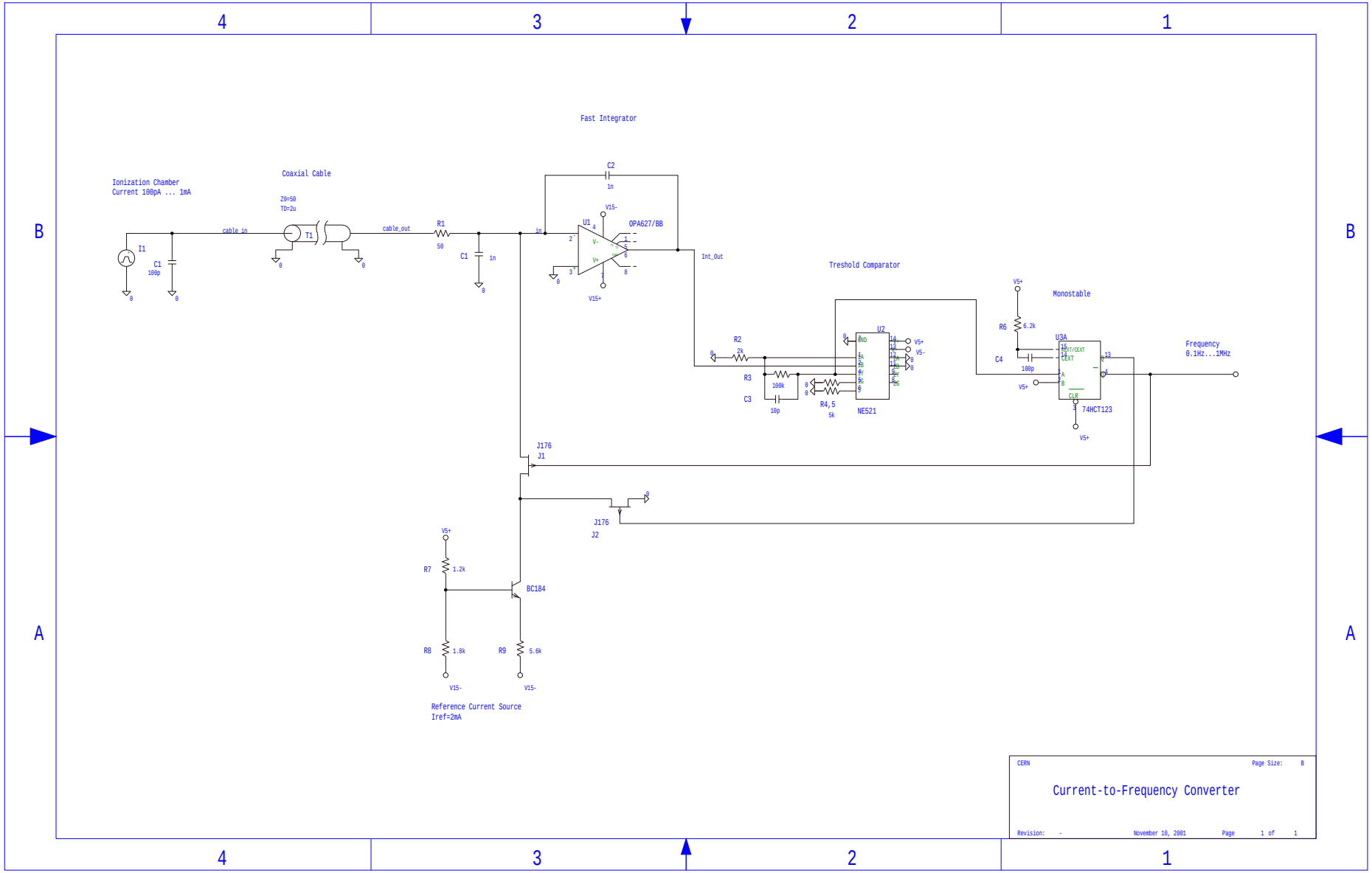
Fast Integrator
Ionization Chamber
Current 100pA ... 1mA
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C1
100p
Coaxial Cable
Z0=50
TD=2u
T1
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cable_out
R1
50
C1
1n
in
C2
1n
U1
OPA627/BB
V15-
V15+
Int_Out
Treshold Comparator
U2
NE521
R2
2k
R3
100k
C3
10p
R4,5
5k
V5+
V5-
Monostable
R6
6.2k
C4
100p
U3A
74HCT123
CLR
Frequency
0.1Hz...1MHz
J176
J1
J2
R7
1.2k
BC184
R8
1.8k
R9
5.6k
Reference Current Source
Iref=2mA
CERN
Page Size: B
Current-to-Frequency Converter
Revision: -
November 10, 2001
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