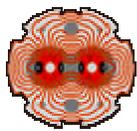


LHC Beam Loss Monitor Threshold Comparator

Design Considerations



Main Tasks of BLMTC

Over the VME-bus:

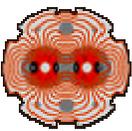
- Establish communication
- Read configuration data with added security
- Send data for storage (post-mortem)

Optical Link

- Synchronise / Demultiplexing of the signals
- Save data in FIFO memories
- Comparison of the received redundant data
- Comparison with the threshold and warning levels

Other

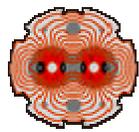
- Read Beam-Energy data / Time-Stamp
- Give software trigger and TTL output for dumping the beam
- Work autonomous (protection against main CPU fail)



Transmission of Data – Codeword

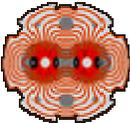
Preamble	Start	Ion Chamber Data	ADC data	Status	Padding	CRC
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Data	min	max	Remarks
Ion.Chamber	72	80	9 Ion chamber data
ADC	64	80	8 or 10 bit ADC per chamber
Position	0	24	3 extra bits per chamber
Preamble	4	24	Used for clock synchronisation.
Start	0	16	Maybe extra S/S will not be needed.
Status*	8	16	Bits showing HT (High Tension).
CRC	17	33	More likely CRC-32 (i.e. 33 bits)
TOTAL	165bits	273bits	



Reliability Increase of Link

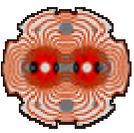
- **Doubling of Transmission Lines**
- **Manchester Encoding**
 - Synchronous transmission
- **CRC (Cyclic Redundancy Check)**
- **Comparison of the signal with its redundant**
- **FAM (Frame Alignment Monitor)**
 - Scan the digital bit stream for a FAW/preamble
- **Inversion of One Signal**
- **Time-Stamp of data**



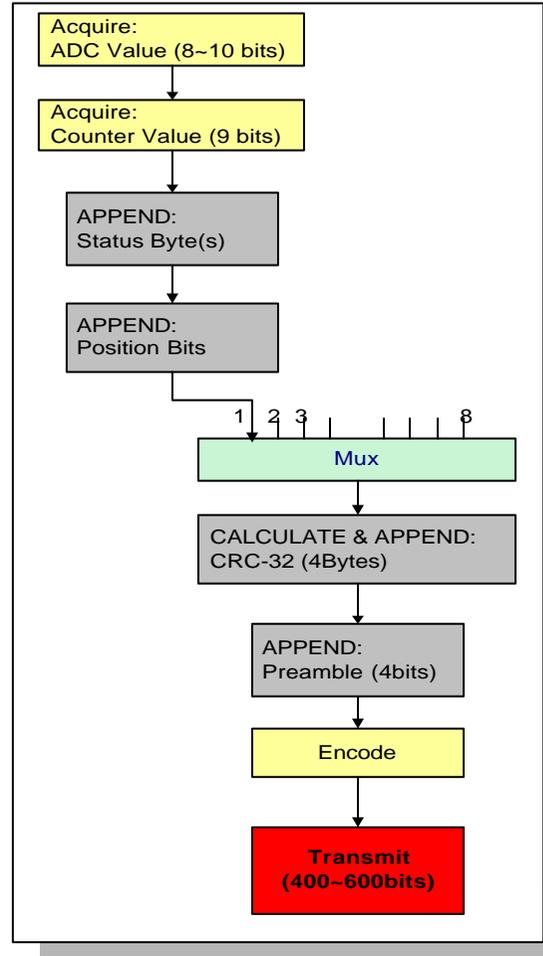
Comparison of Redundant Data

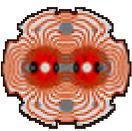
The comparison could be made:

- **At the output level** (i.e. the *Th* & *W* outputs)
 - Masks any differences below
- **Over fixed intervals**
 - Leaves uncertainty
- **At the Sum-Registers level**
 - Much more computation
- **Their CRCs**
 - both messages pass the check and contain identical information
 - 4 bytes only and $\text{Pr} \leq 1\text{E-}20$ (Probability of Non-Detection)



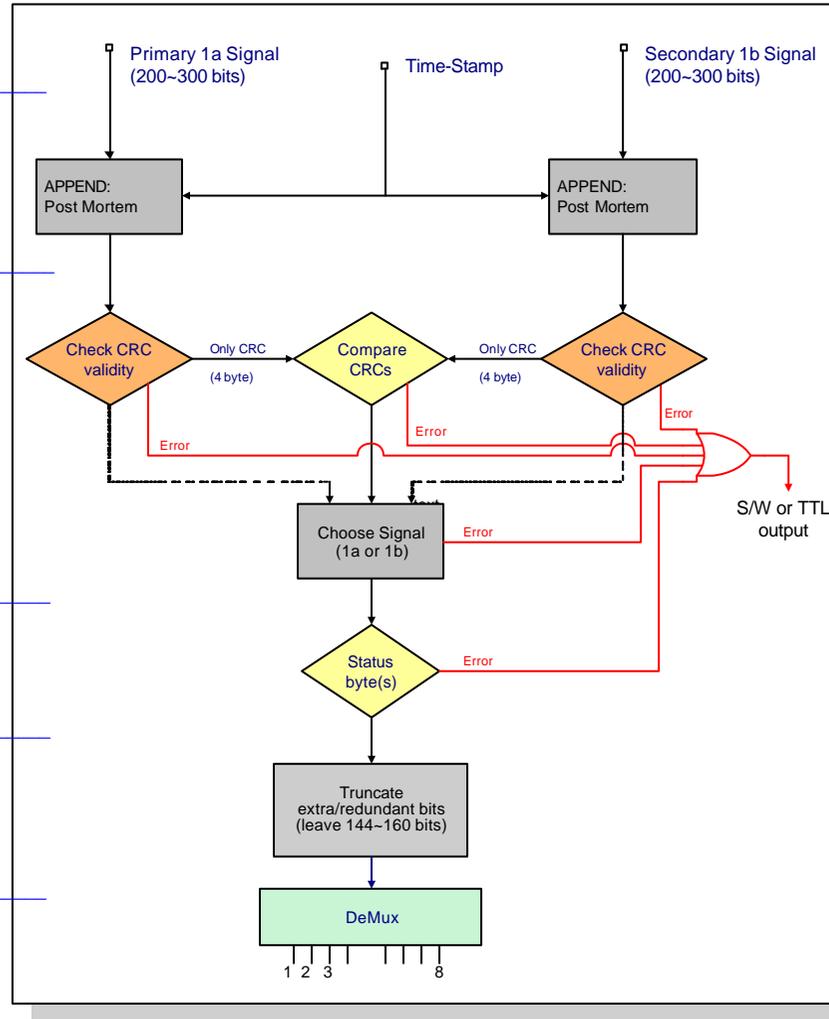
Codeword Production

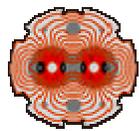




Signal Verification (1)

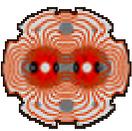
- Reception
- Post-Mortem
- Transmission Check & Signal Choice
- HT Check
- Format Signal



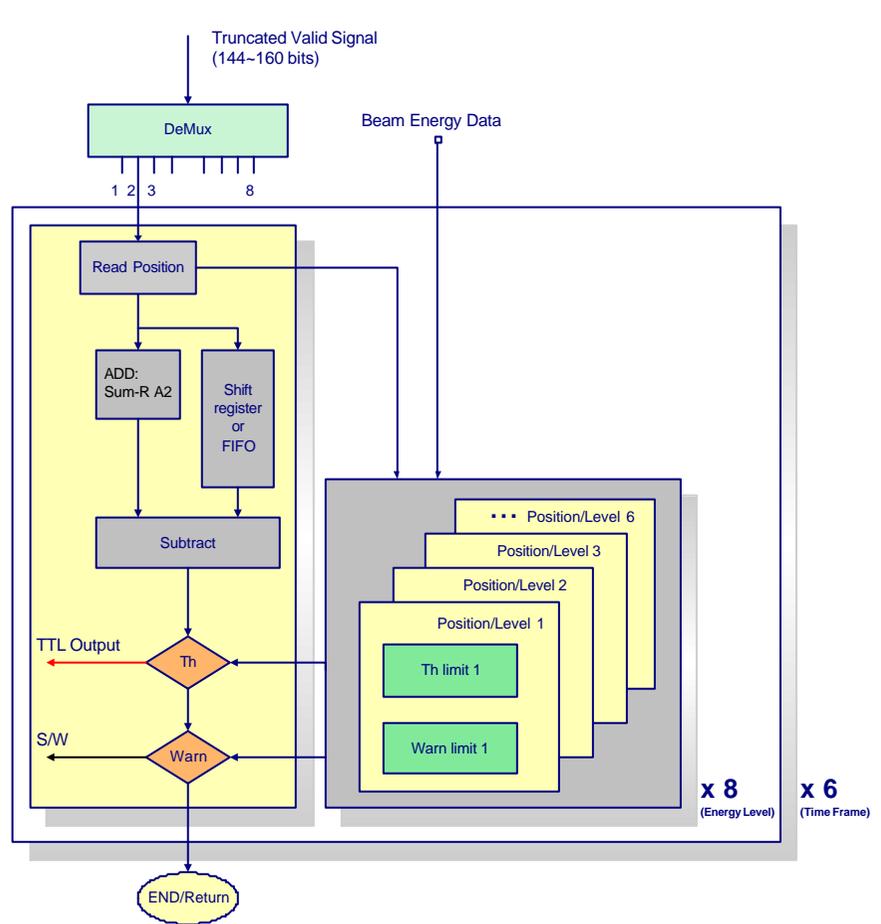


Signal Verification (2)

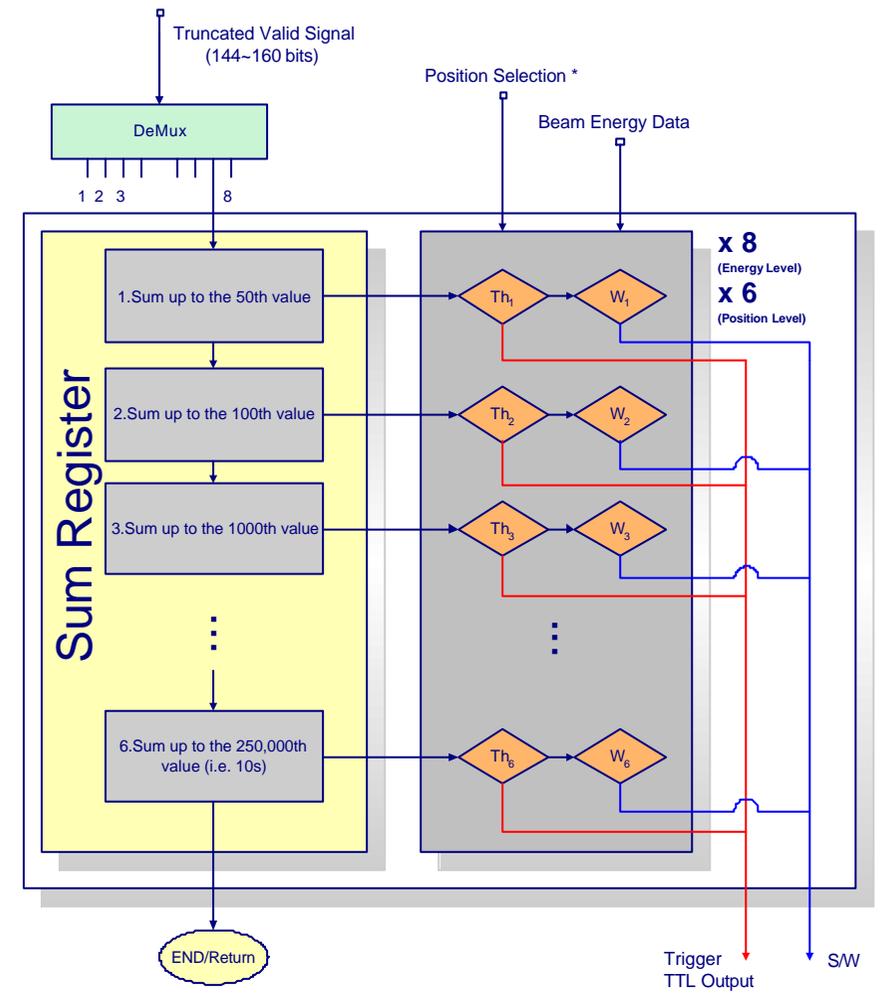
A	B	C	Output	Remarks
0	0	0	Dump	Both signals have error
0	0	1	Dump	
0	1	0	Signal B	S/W trigger (one signal at least has error)
0	1	1	X	Cannot occur / S/W trigger
1	0	0	Signal A	S/W trigger (one signal at least has error)
1	0	1	X	Cannot occur / S/W trigger
1	1	0	Dump	S/W trigger (prob. one of the counters has error)
1	1	1	Signal A	By default (– B signal would be also correct)
*Where A & B: CRC checks, C: Comparison of CRCs, 1:Correct, 0:Error				



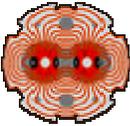
Threshold Comparator



Threshold Comparator System Using Sum-Registers



Threshold Comparator System Using Interrupt Points

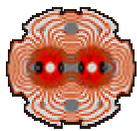


Universal Table Update

- **The threshold (Th) and warning (W) levels are defined by:**
 - **8 Beam Energy Levels (0.45/1 /2/ 3/ 4/ 5/ 6/ 7 TeV)**
 - **6 Position Levels**
 - **6 Time frames**

- **288 pair of values to be loaded universally.**

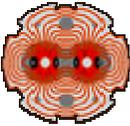
- **Advantages**
 - **One table for all monitors**
 - **Can thoroughly be prepared and checked before it is uploaded.**
 - **Quick and easy upgrade of all systems when it is needed.**
 - **Less computation in each system**



Requirements

For a 10s observation & with acquisition every 40 μ s:

- **FIFO Buffers**
 - **281 KBytes** for Ion.Chamber Data (9 bits)
 - **250 KBytes** for ADC Data (8 bits)
- **Sum – Registers**
 - **27 digits long** register
- **Memory Requirements**
 - System Using Sum-Registers: **9000 KBytes**
 - System Using Interrupt Points: **4250 KBytes**
- **Data Rate**
 - Transmission of 600 bits gives **15Mbps @ 40 μ s acquisition**
20Mbps @ 30 μ s acquisition



Future

- **How the ADC data will be treated.**
 - **0.234 , 22.345 , ...**
 - **When zero counts only.**

- **Speed and capacity of FPGA**
 - **That define the choice of TC**