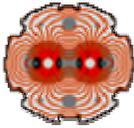# LHC Beam Loss Monitor Threshold Comparator

Design Considerations:

- *Th values storage & update*

- *Beam Energy*

- *Status/Error Information*

- *Identification & Installation Procedures*

Christos Zamantzas

Threshold values storage

- **Non-Volatile RAM on the mezzanine to hold the *Th* table.**

  - ▲ **Specific *Th* to every Ion. Chamber globally.**
  - ▲ **Data always available for reload after a power down or reset.**
  - ▲ **Can be used as a calibration and offset tool.**
  - ▲ **Less computation in each system. (Read vs. Calculated value)**
  - ▼ **Extra electronics**
  - ▼ **More tables to prepare and**
 - ▼ **Must make sure that they are loaded in the right card.**

- **External connector on the surface card to load data.**

- **Assuming that six 16-bit and five 32-bit *Th* values needed per Chamber (i.e. 11 TimeWindows) then:**

  512 bytes per Energy step on every card.

Christos Zamantzas
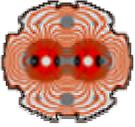
Threshold values update

- **Update from NVRAM into the FPGA**

  - ❑ Should be possible <u>only</u> when no beam circulating?

  - ❑ or anytime?

- **Ways to determine no operation** (i.e. no beam circulating)

  - ✓ BIC interface & Beam Permit Status.

  - ✗ MicroFIP connection in the tunnel. (maybe not available)

  - ✗ VME bus (not reliable)

Christos Zamantzas
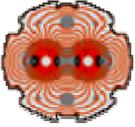
Beam Energy

- **Way to determine wrong or no beam energy transmission**
  - ✓ **BET (Beam Energy Tracking) "status" output.**

- **Steps/divisions needed to describe the energy.**
  - ❑ **8 steps (0.45, 1, 2, … , 7 TeV) ?**
  - ❑ **14 steps (0.45, 1, 1.5, 2, 2.5, … , 6.5, 7 TeV) ?**
  - ❑ **More ?**

Christos Zamantzas
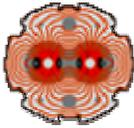
Status Information

- **High Tension – 1 bit per 8 chambers**

- **CFC power – 1 bit per 8 chambers**

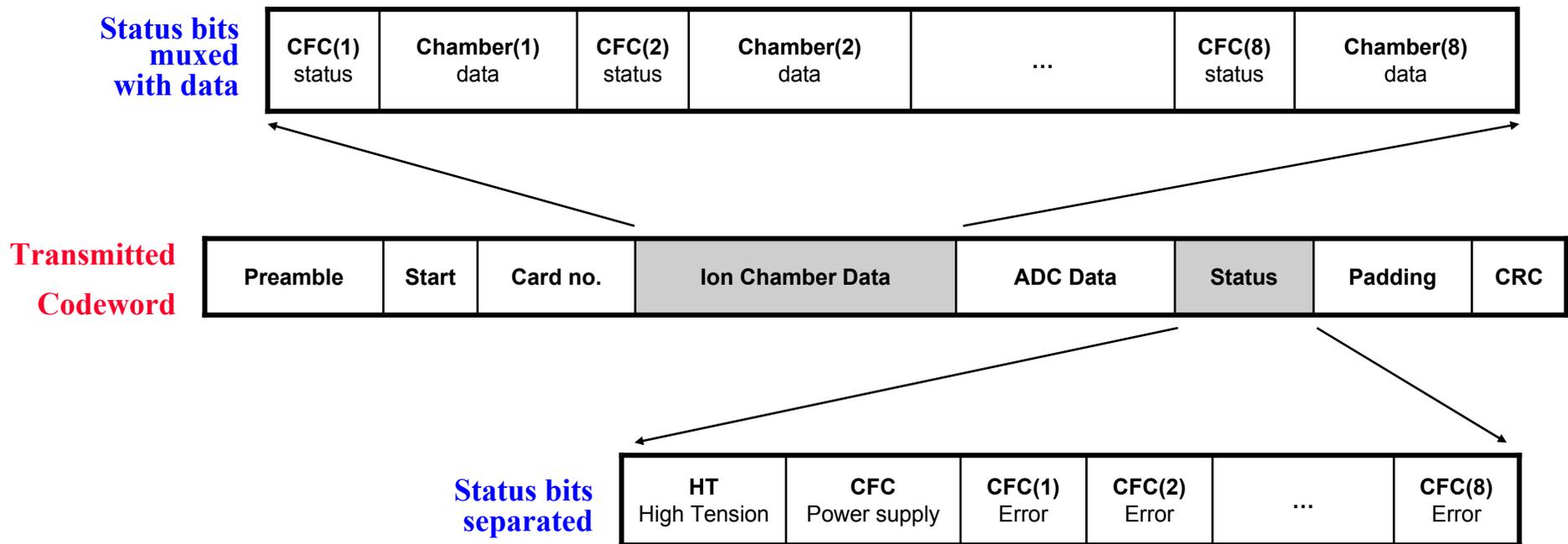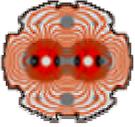- **CFC error – 1 bit per chamber**

- **Laser status possibilities(?)**

Status bits muxed with data

CFC(1) status	Chamber(1) data	CFC(2) status	Chamber(2) data	...	CFC(8) status	Chamber(8) data

Transmitted Codeword

Preamble	Start	Card no.	Ion Chamber Data	ADC Data	Status	Padding	CRC

Status bits separated

HT High Tension	CFC Power supply	CFC(1) Error	CFC(2) Error	...	CFC(8) Error

Figure: Ways to tx status information.

Christos Zamantzas

Identification Procedures

**Ways to identify components to prevent errors from wrong connections:**

- **Tunnel Card no. (10bits) transmission on every frame**
  - ➔ **Equals to giving an ID to each Ionization Chamber.**
    - e.x. (in decimals) chamber 234-7 would mean 7th chamber of card no. 234

  - ➔ **Possibility of comparing that ID with *Th* table's ID.**
    - During the preparation of the table the ID will be added on its top and the FPGA should compare if the table ID is equal to that received from the tunnel card.

- **Setup frame transmission.**
  - ➔ **If bidirectional comm. then with request.**
  - ➔ **With header in the start-up and after a reset.**
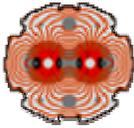
Installation Procedures

- **Make use of the wireless Ethernet connection in the tunnel.**

- **Barcode tags to cards, cables, chambers and position to help cataloging.**
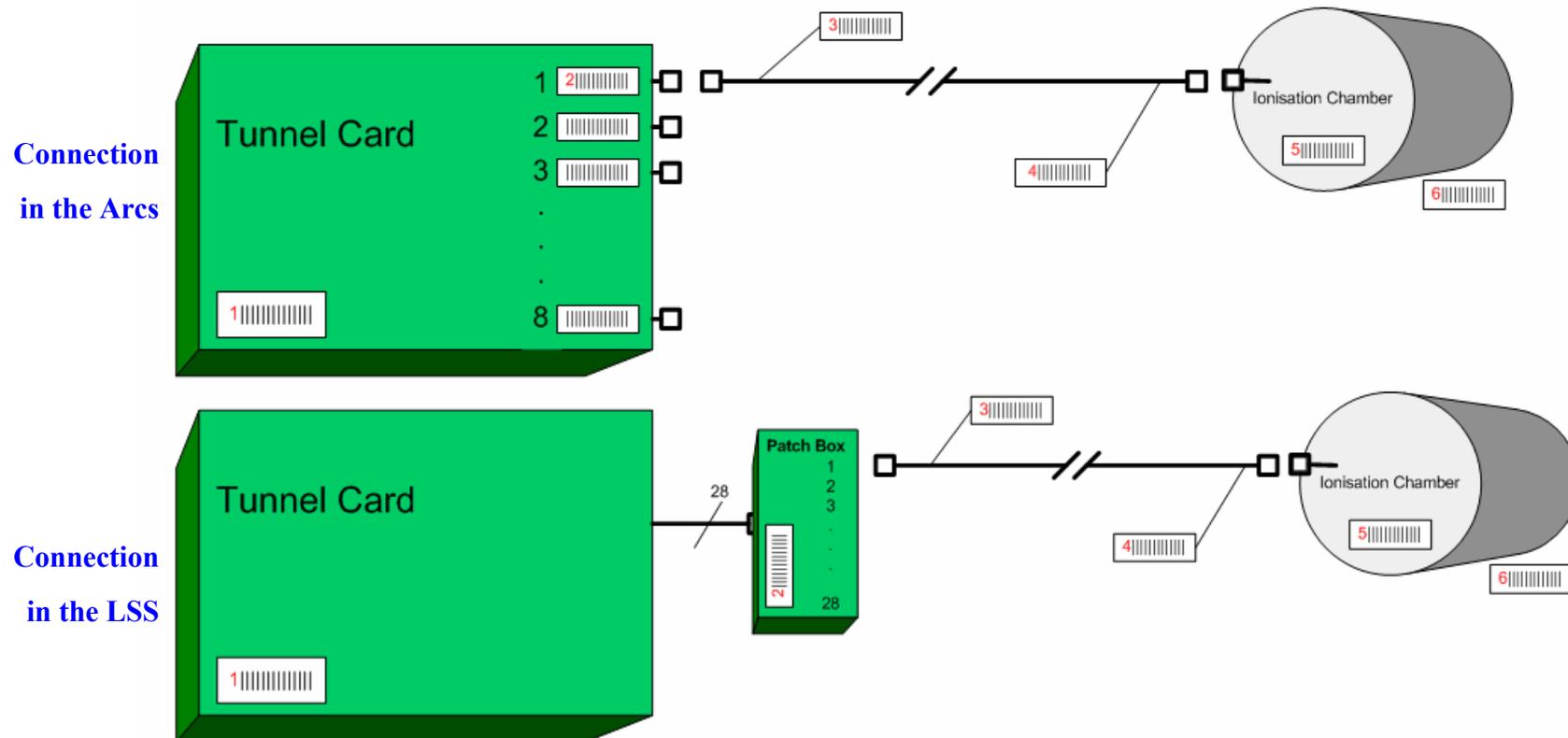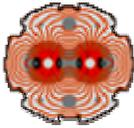
Length of Codeword

Data	min	favourite	max	Remarks
Ion Chamber	64	64	80	8 to 10 bit Ion chamber data (counter)
ADC	64	64	80	8 or 10 bit ADC per chamber
Card no.	0	10	10	565 cards uniquely numbered
Chamber no.	0	0	24	3 extra bits per chamber
Preamble	4	8	24	Used for clock synchronisation.
Start	0	0	2	Maybe extra S/S will not be needed.
Status	1	10	10	Bits showing HT, CFC power and errors.
CRC	17	33	33	Cyclic Redundancy Check/Error Detection
TOTAL	**150 bits**	**189 bits**	**263 bits**	

	200 bits	300 bits	400 bits	500 bits	600 bits
90µs (1turn)	2.23 Mbps	**3.34 Mbps**	4.45 Mbps	5.56 Mbps	6.67 Mbps
40µs	5 Mbps	7.5 Mbps	10 Mbps	**12.5 Mbps**	15 Mbps

Christos Zamantzas