

LHC BLM SINGLE CHANNEL CONNECTIVITY TEST USING THE STANDARD INSTALLATION

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Abstract

For the LHC beam loss measurement system the high voltage supply of the ionisation chambers and the secondary emission detectors is used to test their connectivity. A harmonic modulation of 0.03 Hz results in a current signal of about 100pA measured by the beam loss acquisition electronics. The signal is analyzed and the measured amplitude and phase are compared with individual channel limits for the 4000 channels. It is foreseen to execute an automatic procedure for all channels every 12 hours which takes about 20 minutes. The paper will present the design of the system, the circuit simulations, measurements of systematic dependencies of different channels and the reproducibility of the amplitude and phase measurements.

TEST PURPOSE AND PRINCIPLE

The primary purpose of this test is to ensure the integrity of the cabling of each beam loss monitor. By adding a small harmonic modulation signal on the high voltage supply of the monitors, it is possible to detect a small current on the measurement side (Fig. 1). If anywhere in the signal chain a cable is missing, disconnected or discontinued for any reason, the measurement will not show any harmonic variation of the current.

The second goal is to survey the integrity of the components. The measured amplitude and phase of every channel (monitor or spare) is compared to a predefined threshold measured for every channel. If one of them is outside the limits, the test will fail and the beam permit [1] will not be raised.

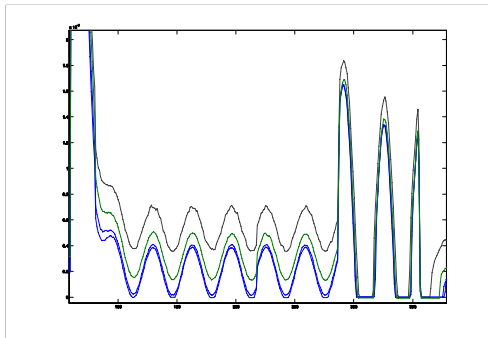


Figure 1: Ionisation chamber signals modulated.

LHC BLM SYSTEM

The LHC BLM system is organised in eight different groups. Each group has a high voltage power supply, which covers two half arcs and one straight section. For each group, there are three or four crates, which can hold up to 256 channels each, connected to one ionisation

chamber (IC) or two in certain case (IC2) or one secondary emission monitor (SEM). Each monitor has a low pass filter with a serial resistor and a capacitor used to store charges. With this structure, the surface power supply can be small. When a beam loss or a variation of the high voltage occurs, charges are moving to the tunnel card BLECF [2]. This card integrates charges for 40µs and sends the result digitally to the surface electronic threshold comparators BLETC [3]. Longer integration windows (running sums) are then computed. When a connectivity test is performed, the processing unit (CPU) sends one of the running sums every second to the combiner and survey card BLECS for analysis (Fig. 2).

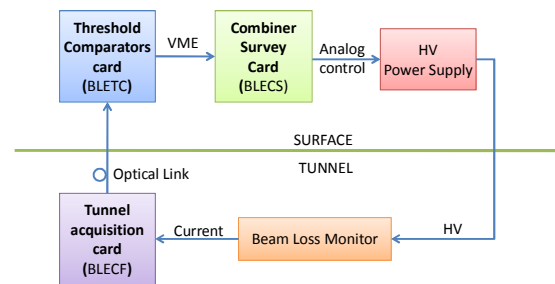


Figure 2: The LHC BLM system viewed as a loop for the connectivity test.

Connection to the Beam Interlock System

The LHC BLM system is connected to the beam interlock system through the CIBUS interface. There are two of these interfaces per point. One is for unmaskable and the other for maskable channels. The BLM system receives from this interface the status of the global beam permits (beam info). The logic used to generate the beam permits includes the results of various system tests including the connectivity test.

Hardware Timers and Test Triggering

The LHC BLM system includes two hardware timers to ensure regular testing of the system. The first timer is linked to the “system test” which includes the connectivity test. The second one is linked to the consistency test [4] which ensures agreement between settings held inside the front-end and in the LSA database. If the tests are not triggered within a fixed time, the next injection will be blocked through the beam permits lines. To allow LHC operation again, the tests have to be triggered and their results need to be satisfactory. When a test is requested by the internal timer, the BLM system raises a status bit and the LHC sequencer (or a manual operation) triggers the test. No test can start if there is beam inside the machine (hardware check of the beam info).

TEST DESCRIPTION

The connectivity test, also called modulation test, consists of adding a small harmonic signal to the control voltage of the high voltage power supply of the monitors (Fig. 1). This variation is propagated to the monitors, which are reacting by generating a current. This variation is measured with the standard acquisition chain (Fig. 2) and the results transferred to the combiner card by the CPU at the nominal rate of one per second. The combiner is performing an analysis of the resulting signal and calculates the peak to peak amplitude of the signal and its phase difference compared to the modulation introduced in the system.

Simplified Equivalent Circuit

The equivalent circuit of the system is shown in Fig. 3. The high voltage supply is connected to the detector through an 11 MΩ resistor. The parallel capacitor (C filter) is used as a supply of charges when a fast loss occurs. The IC or the SEM is represented by a capacitor. The input circuit of the tunnel card is represented as a resistor and capacitor, the virtual ground of the integrator is represented as a shunt resistor. The contribution of the cables capacity and resistivity is small compared to the component values for the frequency range (1 mHz to 1 Hz); they are ignored for this simulation.

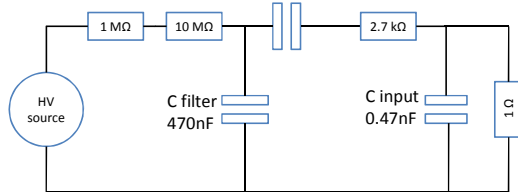


Figure 3: Simplified equivalent circuit.

Simulation Results

The simulation of the equivalent circuit shows the behaviour of the system depending on the harmonic frequency injected in the system (Bode diagram Fig. 4 and 5). The goal is to find a good working point to test the integrity of the cabling. We are also interested in the dependence of this diagram to the variation of the key component values: The monitor capacity (Cmonitor), as it varies with the monitor type, and the Cfilter, as it is directly under a lot of stress (radiation) and may lose its capacitive property.

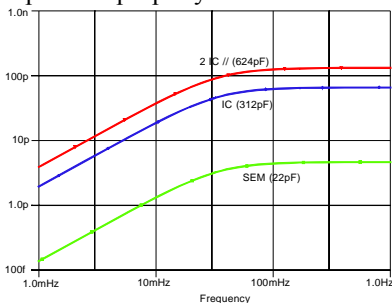


Figure 4: Magnitude of the Bode diagram for the 3 monitor types (SEM, IC and 2 IC in parallel).

The working frequency of 0.03 Hz was selected as it gives the best sensitivity (in phase) for a variation of the Cfilter (Fig. 5) with small magnitude changes (not shown). In Fig. 4, the magnitude of the signal at this frequency is nearly optimal and the monitor type can easily be distinguished. The variation of Cmonitor doesn't contribute at all to the phase change (not shown).

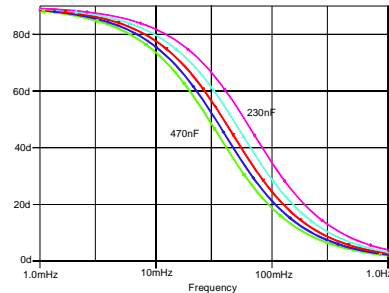


Figure 5: Phase of the Bode diagram for different values of the Cfilter.

Implementation of the Test

The generation and the processing of the test are done inside the combiner and survey card. When a test is triggered, the field programmable gate array (FPGA) starts generating the modulation signal added to the high voltage. The CPU provides the measurements every second to the card for processing. Once the complete set of the 256 channels has been written, the amplitude and the phase are calculated using the cross correlation between the measured signal and the initial recorded modulation.

Threshold Comparison and Results Availability

When the results of the test are available, they are compared to the channel specific thresholds to compute final passed/failed information for each channel. A global status with the 256 channels of the crate is being used to generate the beam permit signal.

The results of the test are automatically logged to the LHC logging system and are available shortly after the end of the test.

MEASUREMENTS ANALYSIS

An analysis of the behaviour of the system has been conducted to validate the test. The results are also used to produce thresholds to be loaded inside the front-end for the automatic test.

Data Retrieving

The measurements and the status generated by the electronics (pass/failed for each channel) are automatically stored in the Measurement database, from where they are sent to the Logging database without filtering for long term availability. The information is grouped per threshold comparator card and per crate. To link a channel to a detector name, the Layout database is accessed. To know if a channel is connected to the maskable or unmaskable beam interlock interface, the LSA database is accessed.

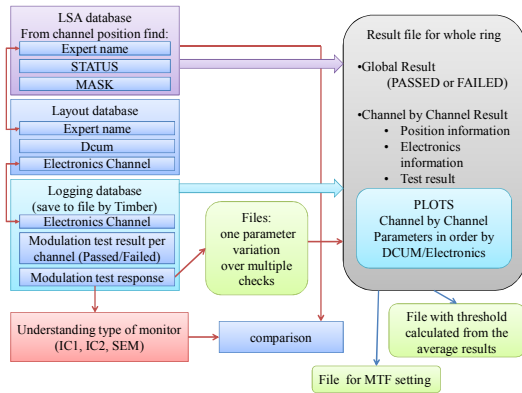


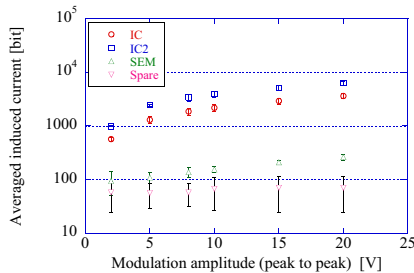
Figure 6: Overview of the analysis for system validation, parameter optimisation and threshold calculation.

Detector Recognition

The type of the detector can be identified as shown in the simulation by looking at the level of the induced current. By applying a simple rule it is possible to place the channel into four categories. Fig. 7(a) shows that starting from a modulation voltage of 8V, the SEM, the IC, the double IC (IC2) and the SPARE channels are clearly identified and not overlapping.

This detector identification is compared with the database expert name and appears in the report.

(a)



(b)

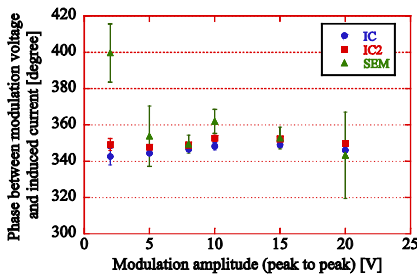


Figure 7: Average induced current (a) and phase (b) versus different modulation amplitudes. Data are collected from the LHC point 8 right and straight section including spare channels.

Modulation Voltage Optimisation

In order to optimise the harmonic modulation voltage control, different settings were studied. The variance of the harmonic induced current for the three different detector types and the spare channels (unconnected) are shown in Fig. 7.

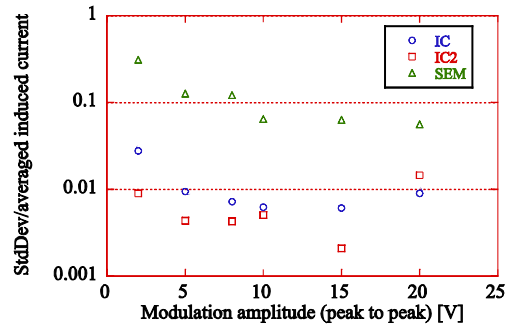


Figure 8: Measurement reproducibility versus modulation amplitude. Different options are being investigated to reduce the SEM error.

The SEM signal shows a large variance at low voltage, since the absolute value of induced current is very small. For 15V and above, the error increases for IC (and IC2) probably due to saturation effects. We chose 10V for the modulation amplitude for good S/N ratio and reproducibility of measurement for all monitor types.

Thresholds Production

The individual thresholds, to be set inside the electronics for each channel, are the minimum and the maximum boundaries for the harmonic induced current and the phase. To calculate them, the average value over multiple measurements for each parameter (Fig. 7) is taken and a 15% margin (Fig. 8) is added.

SUMMARY

The BLM system of the LHC is now capable of self testing its connections and removing ambiguities due to cabling malfunction. The system sensitivity and measurement reproducibility (better than 1% for the IC and 5% for the SEM) exposed in this paper allows the distinction between monitor types and different setups. Component value changes due to radiation or ageing can be detected with high sensitivity. The threshold comparison automatically blocks beam injection in case of system nonconformity.

REFERENCES

- [1] Engineering Specification, "The Beam Interlock System For The LHC", LHC Project Document No. LHC-CIB-ES-0001-00-10, version 1.0, 17-02-2005.
- [2] B. Dehning, E. Effinger, J. Emery, G. Ferioli, C. Zamantzas, "Single Gain Radiation Tolerant LHC Beam Loss Acquisition Card", Proceeding of DIPAC'07, Venice-Mestre, Italy.
- [3] C. Zamantzas, B. Dehning, E. Effinger, J. Emery, G. Ferioli, "The LHC Beam Loss Monitoring System's Surface Building Installation", Proceeding of LECC'06, Valencia, Spain.
- [4] C. Zamantzas, B. Dehning, J. Emery, J. Fitzek, F. Follin, S. Jackson, V. Kain, G. Kruk, M. Misiewicz, C. Roderick, M. Sapinski, "Configuration and Validation of the LHC Beam Loss Monitoring System", these proceedings.