Development of a New Data Acquisition System for the Fermilab Beam Loss Monitors

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Abstract— A new digitizing and data acquisition system for the beam loss monitors is being developed for use in several accelerators of the Fermilab complex. In addition to providing diagnostic information about beam loss, the loss monitor system is designed to provide a primary protection against damage to the superconducting magnets of the Tevatron. Protecting the Tevatron magnets over the full set of Collider operating conditions requires the abort logic and thresholds to be flexible and reconfigurable quickly from stored settings. A digitizer card is the core component of the system. It integrates and digitizes the current from the loss monitor chambers each beam revolution period (21 μs), maintains three running sums of up to 64k measurements, and compares the measurements and sums to programmable abort thresholds. In this paper we report on the overall system design and on tests of a prototype digitizer card during Tevatron operation.

***Index Terms*— Current measurement, Data acquisition, Dosimetry, Ionization chambers, Integrators, Radiation detectors.**

I. Introduction

A new digitizing and data acquisition system for beam loss monitors (BLM) is being developed for the accelerators of the Fermilab complex. In addition to providing diagnostic information about beam loss, the system is designed to provide a primary protection against damage to the superconducting magnets of the Tevatron. Beam losses are detected using the ion chambers that were installed when the Tevatron was built. The chambers have proven robust and have the appropriate dynamic range [1]. The data acquisition system designed in 1981 has served reliably for accelerator diagnostics and protection during fixed-target operation. However, the beam abort logic in the original system was not designed to deal with the variety of operating conditions during collider running. Protecting the Tevatron magnets over the full course of injection and operation requires the abort logic and thresholds be customized for the different accelerator operating states. Since it takes about 24 hours to accumulate the antiprotons for a store, false aborts carry a heavy penalty in lost running time. At present, the loss-monitor abort is disabled as soon as the antiprotons are injected and protection is based on the Quench Protection Monitors which have a response time of about 16 ms.

The FNAL Booster and Main Injector will also employ the new BLM system. These machines are the work horses of the Fermilab program, and measurements of beam loss are important to avoid activation of equipment that would render it unserviceable. The method of integration in the new system is linear. This approach makes use of digital signal processing available in the programmable logic and allows different accelerators with different cycle times to use a common system hardware.

The new BLM system uses a standard 6Ux160mm VME format with a custom J2 backplane for local system communication. This J2 backplane is referred to as the BLM Control Bus. Besides the VME crate computer in Slot 1 that communicates data to the main control system, the BLM system consists of Integrator/Digitizer Cards, a Timer Card, a Control Card, and an Abort Concentrator Card. Each of these is described in the following sections.

II. The BLM System Electronic Cards

A. Integrator/Digitizer Card

The Integrator/Digitizer Card (DC) integrates and digitizes the current from four loss monitor chambers each beam revolution. To avoid dead time between measurements, signals for each input are switched between the two channels of a TI/Burr-Brown ACF2101 integrator chip. Results are digitized from the two channels on alternate cycles and fed to on-board programmable logic devices.

The digitizer has a 16 bit resolution. Scaling is such that one digitizer count represents 15.26 fC of charge in the integrator. The sensitivity of the BLM ion chamber is approximately 70 nC of charge per Rad.

The logic maintains three running sums per channel with programmable durations of up to 65,536 base clocks (1.4 seconds for the Tevatron) and compares the current measurement and the running sums to abort thresholds (4 thresholds in all). Each threshold can be set independently for each channel. There can be up to 16 digitizer cards in a crate. We envision sliding sums with periods of approximately 1 ms,

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50 ms and 1 s for normal operation. The block diagram in Fig. 1 illustrates the signal processing for each channel. Note that the Sum registers will be read and the Threshold Registers written over the BLM Control Bus. The SRAM memory which stores the integrator output values can be read over the VME bus (J1) by the crate computer.

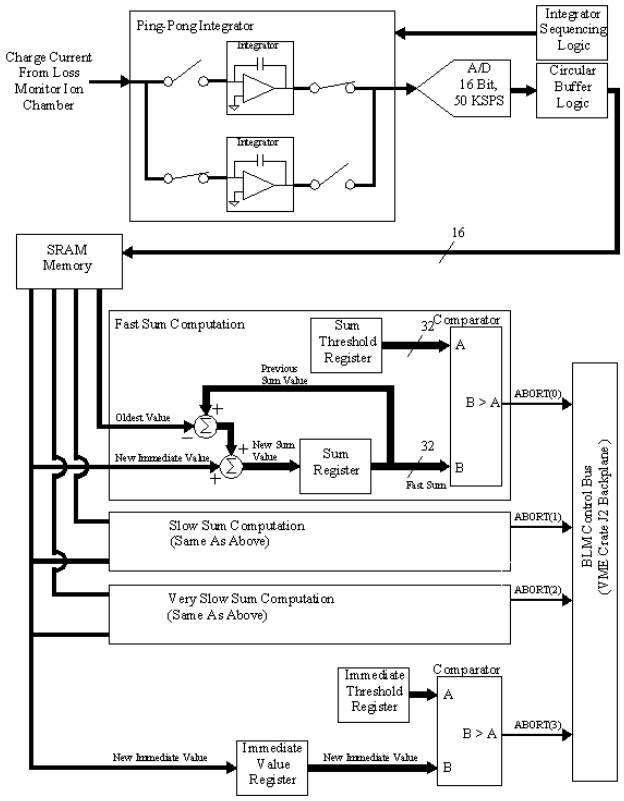

Fig. 1. Block diagram of the signal processing for one of the four channels on the Integrator/Digitizer Card.

B. Timing Card

The Timing Card (TC) receives Accelerator system wide timing information from three sources, the Tevatron Clock, (TCLK), the Beam Sync Clock (BSYNC) and Machine state Data (MDAT).

The TC decodes BSYNC to generate the 21μs BLM system master clock which it distributes on the BLM Control Bus. The TC maintains a 64K circular buffer of timing information for each cycle including a 32-bit time of day and a 24-bit microsecond counter which is reset at one second intervals; this buffer is in parallel with the circular buffer of loss measurements in the Digitizers. The master clock defines the integration interval of the Digitizers and sets the threshold-comparison timing and abort-logic comparison timing. The TC also generates signals at appropriate intervals to cause the Digitizers to latch the current values of the sliding sums and the Controller Card to read these sums with the latched timing information.

The TC decodes TCLK and sends a signal to freeze the data buffers in the Control card, Timing Card and Digitizers in the case of an abort. Other events from TCLK are used to signal the BLM system to collect and store synchronous ring-wide data samples for beam studies. The MDAT signal is decoded to determine the machine state and generate an interrupt to the Control Card causing it to load the appropriate abort thresholds and logic when the Tevatron machine state changes.

C. Control Card

To ensure that data communications and other tasks running on the VME crate computer do not impact the reliability of the BLM abort logic, the Control Card (CC) provides an independent dedicated processor that manages the setting of abort thresholds and other parameters used in the abort logic. The CC communicates with the other system cards over the dedicated custom J2 backplane keeping local communications separate from VME data transfers. The CC also maintains circular buffers that store the histories of the three running sums for each digitizer channel with time stamps provided by the TC. The histories will be at least 4096 time bins deep. The history can be read out via VME either on command from VME crate computer or saved in response to an accelerator control signal. The CC also stores abort thresholds for each of the sums for each channel for up to 256 machine states.

When a change in accelerator state is detected, the CC updates the thresholds in the digitizer cards as well as the abort masks and multiplicity requirements in the Abort Concentrator Card.

D. Abort Concentrator

The four abort signals from each channel on each Integrator/Digitizer Card are read by the Abort Concentrator Card (AC) every 21μs integration interval. The aborts of a particular type are counted and compared to a programmable multiplicity requirement for that abort type. It is possible to mask channels off in the AC so they do not participate in the count. If the multiplicity for that integration interval equals or exceeds the threshold, a beam abort signal is generated. This logic is illustrated in Fig. 2.

To accommodate the different operating conditions, the abort masks and multiplicity thresholds in the Abort Concentrator can change depending on the Machine State. We have also included a serial link on the Abort Concentrator to allow a single point to receive information from all the BLM crates around the ring to be able to implement a ring-wide abort condition.

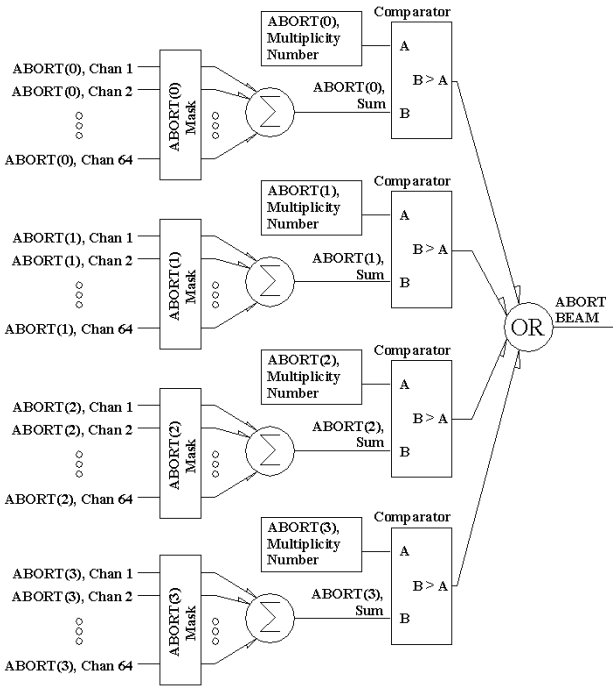

Fig. 2. Block diagram of the abort multiplicity logic on the Abort Concentrator Card.

III. Field Test of the Prototype Integrator / Digitizer

A. Test Description

We built a two-channel prototype version of the Integrator / Digitizer Card in order to test the new integration scheme with actual beam-loss signals from BLM detectors in the Tevatron, Main Injector and Booster. Integrator output data was sampled and recorded for each 21 µs integration interval. The data output of the card was processed and displayed using oscilloscope emulation software written in Visual Basic. The prototype was connected to 21 BLM detectors in the Tevatron, 24 in the Main Injector, and 3 in the Booster. With beam running in each of these machines both large and small beam losses were recorded.

B. Noise Management

The testing provided experience with the noise that will need to be addressed in the final installations. In these initial field tests the bandwidth of the integrator inputs were relatively wide. Input time constants were in the range of 5 µs to 50 µs depending on the installed BLM cable lengths. When the integrator channel was not connected to a BLM, noise levels for the circuit by itself were on the order of five counts RMS (76.3 femto-coulombs), or 1.1 µRad.

With the Integrator/Digitizer Cards connected to BLM signal cables in the service buildings, the frequency content of the noise was obvious in a plot of the test data. Noise at frequencies of 60 Hz and 720 Hz was common. The majority of the noise encountered appeared as common mode. Experiments using several different common-mode chokes connected in series with the BLM signal cables were performed. The chokes consisted of several turns of coaxial cable wrapped on one to three inch donuts made of high permeability material. These chokes were found to be quite effective in attenuating the large common-mode component of the noise while not affecting the input bandwidth of the desired signal to any noticeable degree [3].

Beyond the common-mode noise, significant differential-mode noise signals were observed in several of the BLM detector measurements. Reductions in this component of the noise can be accomplished in two ways. First, the input bandwidth can be narrowed by installing higher values of series resistance before the integrator. Second, further noise reduction is accomplished when the individual integrations are summed into the three time scales used in the abort decision discussed previously. Fig. 3 is a plot of a single measurement made on a Main Injector BLM, and shown for different length sums (smoothing). The cables in the Main Injector can be long, up to 200 m, and can pick up a considerable amount of noise. The cable length also has an impact on the bandwidth of the measurement.

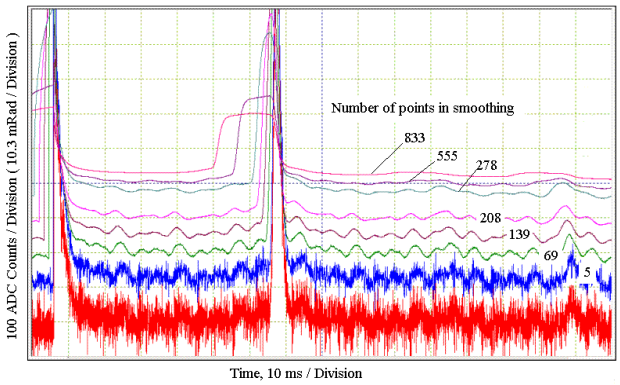

Fig. 3. Plot of the data from a Main Injector BLM showing the effects of data smoothing. Data samples were taken at 47.6 kHz.

Fig. 4 is an example of the effect of the common-mode choke and the effect of reducing the input bandwidth by increasing the input series resistance. This measurement was made on a Booster BLM with a cable that is only 40 m long and hence gives a wider measurement bandwidth compared to the measurement in the Main Injector shown in Fig. 3.

From what we have learned about the noise issues it has been decided that the new BLM system will include a filter box between the BLM signal cables and the Integrator/Digitizer Card inputs. The filter box will include the common-mode chokes and a series resistor whose value will be chosen to produce a standard input time constant given the length of the particular BLM cable run. In choosing the

standard input time constant there is a trade-off between the time resolution of the measurement and the magnitude of the instantaneous loss the integrator will be able to measure without saturating. Exactly where to set this is still under investigation.

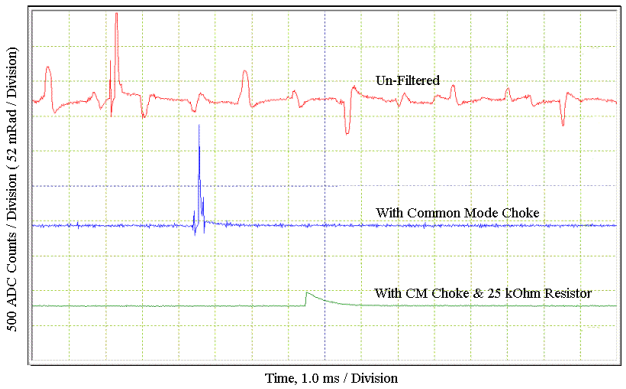

Fig. 4. Plot of the data from a FNAL Booster BLM showing the effects of a common-mode choke and additional input series resistance. Data samples were taken at 47.6 kHz

IV. Summary

By linearly integrating and digitizing charge from the detectors every 21 μs, the new data acquisition system for the Fermilab beam-loss monitors will provide a greater flexibility in the time scales over which losses are monitored and thus allow the use of common hardware for machines with different cycle times. By employing the computational speed of available FPGA programmable logic devices, three sliding sums for each of four channels per module can be computed and compared to programmable thresholds each integration interval. The thresholds can be automatically adjusted according to the particular operating state of the accelerator. If a particular channel's sum is determined to be above threshold an abort status bit is set. A predetermined, automatically adjustable number of abort status bits will be required to be set before an actual beam abort signal is issued.

In the initial tests that have been made we have been able to observe the operation of the new integration scheme. We have also learned of the noise issues in the field and determined techniques for managing them.

References

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