LINEARIZING THE RESPONSE OF THE NSRL SYNCHRONOUS RECYCLING-INTEGRATORS*

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Abstract

The Lawrence Berkeley National Laboratory (LBNL) designed recycling-integrators used for the NASA Space Radiation Laboratory (NSRL) dosimetry feature excellent linearity. However, switching transients in the balancing source add a duty-cycle dependence to the response that manifests as a non-linearity near mid-scale and a slope-change above mid-scale. The onset of this non-linearity limits the typical usable dynamic range. Measurements during a recent run showed that at higher intensities the recycling-integrators would operate in the non-linear region enough to exceed the desired tolerance and over count the dose. This report will show how a FPGA, which implements the scalars, was used to compensate the non-linearity allowing higher dose-rates by effectively doubling the dynamic range of the dosimetry system.

INTRODUCTION

The NSRL dosimetry system uses 23 LBNL designed 16-channel recycling-integrators (9U VME) cards. They are modified synchronous versions of the recycling-integrator that were used at the BEVALAC Biomedical Facility. Other modifications include gain and bias DACs as well as the ability to selectively feed an external calibration source to each channel. An onboard "simulated beam" feature will simultaneously drive a 100nA current (trough the ion-chamber) into all the channels. The recycling-integrators feature a conversion rate of 10pC/count as well as excellent long-term stability. A Xilinx Spartan-II FPGA implements both a 32-bit scalar and preset-scalar for each channel. Two "real-time sums" are also implemented. Each real-time sum feeds a scalar and preset-scalar with the sum of any combination of the board's 16-channels. The FPGA also performs an "auto-bias" function that maintains an offset of 10pA or 1count/sec.

Presently dose cut-off is determined using one of three ion-chambers. Each chamber is made of three foils: a 32-zone concentric-ring/quadrant foil, a high-voltage foil, and a 2-zone concentric-ringed foil [1]. Figure 1 shows that the recycling-integrators become non-linear above 3.5μA. The large 32cm x 32cm element of the 2-zone foil regularly operates in this region. Uncorrected the dose would be over counted by more than 10%. So far this element has not been used for dosimetry. Typically a real-time sum of the 4 inner rings of the concentric-ringed foil is used to create the end of dose cut-off. The current from

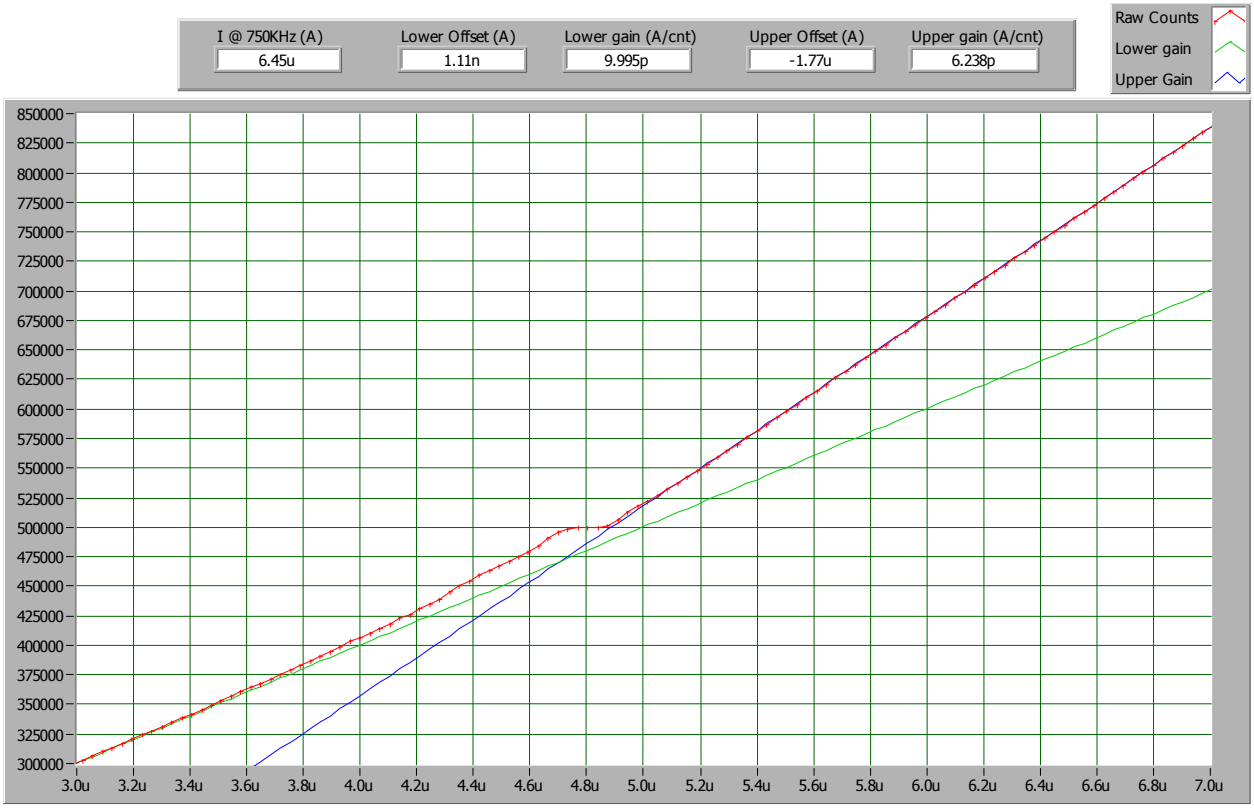

Figure 1: Response of a typical recycling-integrator channel; the dashed lines illustrate the slope-change.

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the 4th ring averages 121nA and therefore has not affected current experiments. Most exposures are done at low intensities (less than 2Gy/min). At 2Gy/min the 4th ring quadrant current is 301nA. The ion-chambers are not directly used to read dose but are calibrated against an industrially calibrated EG&G ion-chamber at the sample isocenter [2]. There is also a fourth ion-chamber having 256-elements, arranged as a 16x16 array, but it is presently not used to create cut-offs.

Since some exposures are done at higher intensities (20-70Gy/min) it was considered necessary to study the non-linearity to see at what point and to which extend it affects the dosimetry.

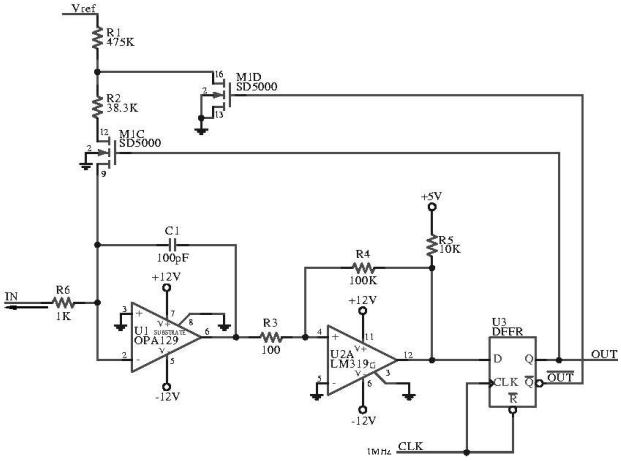

Figure 2: Simplified Recycling-Integrator Schematic

RECYCLING INTEGRATOR

Basic Principles

A recycling-integrator is charge balance converter also known as a current to frequency converter (I/F). Figure 2 shows a simplified schematic of the NSRL recycling-integrator. This circuit measures negative current – flowing out of "IN." A charge-balance converter integrates current (or builds up charge) until a threshold is reached and then fires a balancing current-source for a fixed time to try and bring the total net charge to zero. The integrating capacitance and actual comparator threshold are not that critical, in this case 100pF and 0V respectively. It's the balancing-source and the effective balancing charge delivered that is most critical. Ideally this circuit will attempt to deliver 20µA for 500nS or 10pC/count. In reality, the charge injected by the MOSFETs during switching and the limited response-time of the op-amp affects the effective balancing charge significantly (see figures 3 to 5). The parasitic effects limit the maximum clock rate of the recycling-integrator too less than 1MHz. To compensate, the current and pulse-width are both programmable. The clock pulse-width feeding the flip-flop determines the balancing pulse-width and is global to all channels on a card. Individually programmable voltage reference (Vref) and resistors R1 and R2 determine the balancing-current.

Asynchronous vs. Synchronous

In an asynchronous recycling-integrator the balancing source fires as soon as the threshold is reached. During each charge-balance cycle the total net charge returns to zero and the output frequency varies continuously. For instance, 750KHz would be output as one pulse every 1.33µs. In a synchronous design the balancing-source can only fire when clocked. Since the balancing-source has to wait for the clock, the charge may not get completely balanced within one cycle and will carry over into the next charge-balance cycle; it can take multiple cycles for charge to balance. See [3] for a good description. The frequency varies in discrete steps. In this case, 750KHz would be output as 3 pulses spaced 1µs apart repeating every 4µs.

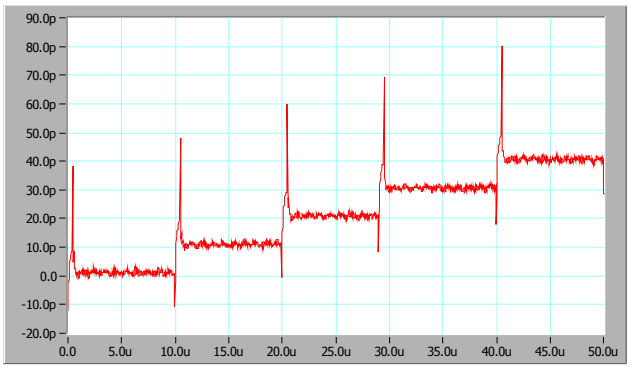

Figure 3: 10pC steps for 10us spacing

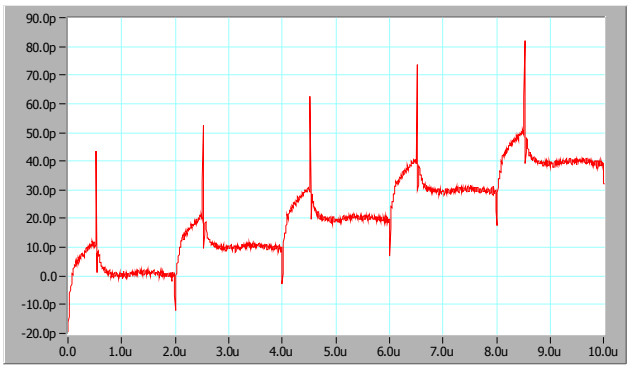

Figure 4: ~9.8pC steps for 2us spacing

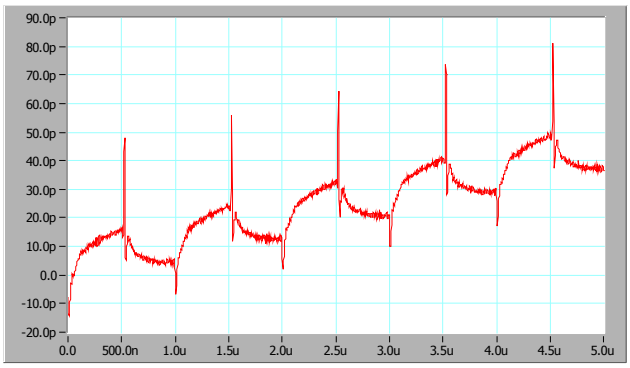

Figure 5: ~8pC steps for 1us spacing

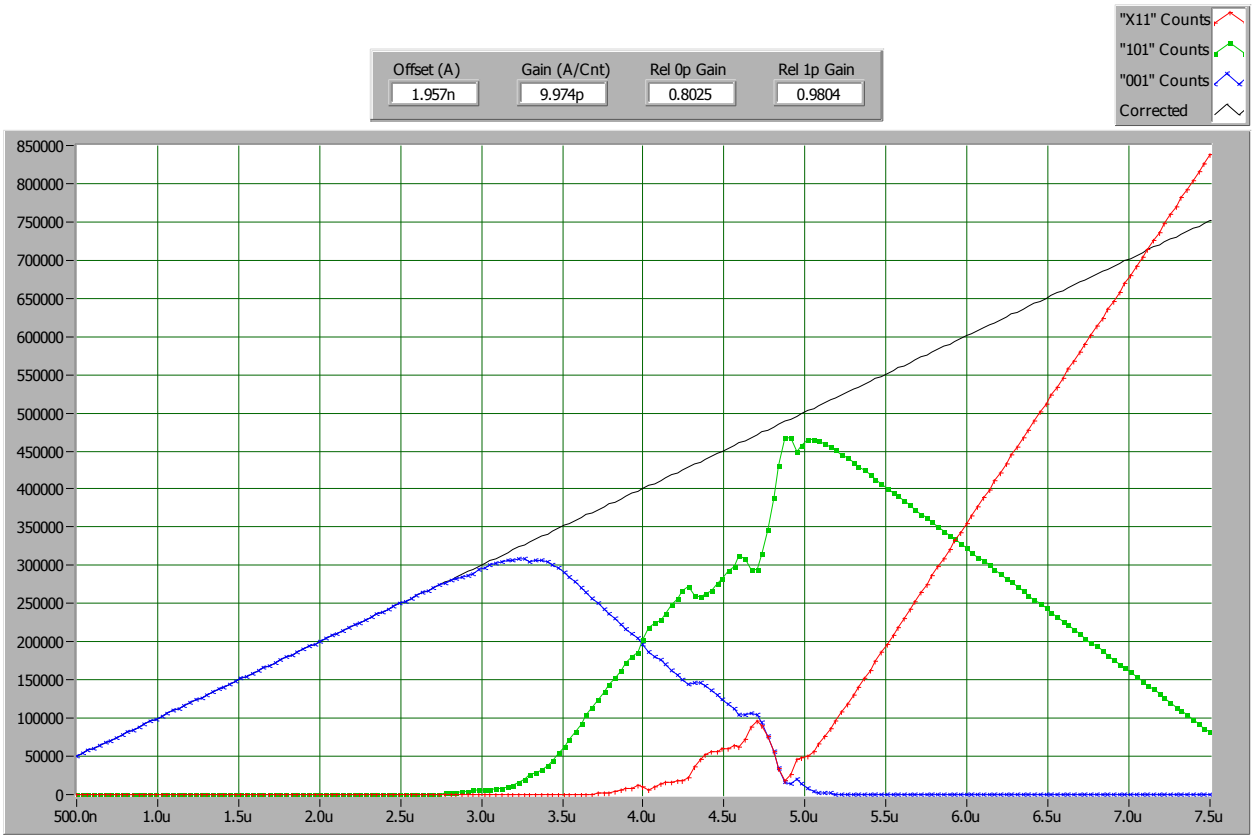

Figure 6: X11, 101, 001 pattern counts; the dashed line is the corrected response.

Non-Linearity

Figures 3 to 5 show that the effective charge-steps delivered by the balancing source decreases as the pulses become closer spaced. At 1µs (fig. 5) they no longer look like steps. What makes linearization possible is that the circuit itself is still operating linearly; the effect of the input current is independent of the effect of the balancing source and superposition still applies. Figure 3 to 5 were generated from the measured integrator voltage minus the assumed ideal integration of the calibration source.

The discrete nature of synchronous recycling-integrator causes the non-linearity to set in earlier than an equivalent asynchronous design. However, since the non-linearity is caused by the switching action and the timing is fixed, the discrete nature also provides the information need to correct the linearity.

BIT-STREAM LINEARIZATION

A synchronous recycling-integrator is also a first-order delta-sigma modulator and the output is then a bit-stream: 1 for a pulse, 0 otherwise. A repeating 0111 pattern is then another way to represent the 750KHz output. In this notation the rightmost bit is the present bit; the bits to the left are the previous samples. By interpreting the bit-stream it's possible to correct the linearity. Pulses that arrive without a pause (11 pattern) only deliver ~8pC per pulse. If only one pause separates pulses (101 pattern), then ~9.8pC is delivered. If these factors are applied to the repeating 0111 pattern, then the correct current can be determined. The pattern produces one match to the 101 pattern and two matches to the 11 pattern, or 9.8pC + 2x8pC = 25.8pC. Over the 4uS period this is equivalent to a current of 6.45µA, which agrees with figure 1.

FPGA Based Linearization

A 20-bit accumulator was added to the FPGA to keep track of fractional counts. Depending on the pattern a relative gain factor for 0-pause or 1-pause pulse is added: typically .8 or .98 respectively. The actual values vary from channel to channel and are stored in registers. Figure 6 shows the resultant correction.

CONCLUSION

This solution is able to linearize the recycling-integrators over their full range to less than 0.07% error. Lowering the sampling clock to 700KHz could reduce the linearity-error but not to this extent.

REFERENCES

[1] "NSRL Manual," pp. 19-23.
[2] J.R. Alonso, et al, "Operations Experience at the BEVALAC Radiotherapy Facility," in PAC'81, 1981, p. 2827.
[3] Analog Devices, "AD652 - Monolithic Synchronous Voltage-to-Frequency Converter," Rev. C, 2004, pp. 6-8.